FIG. 1

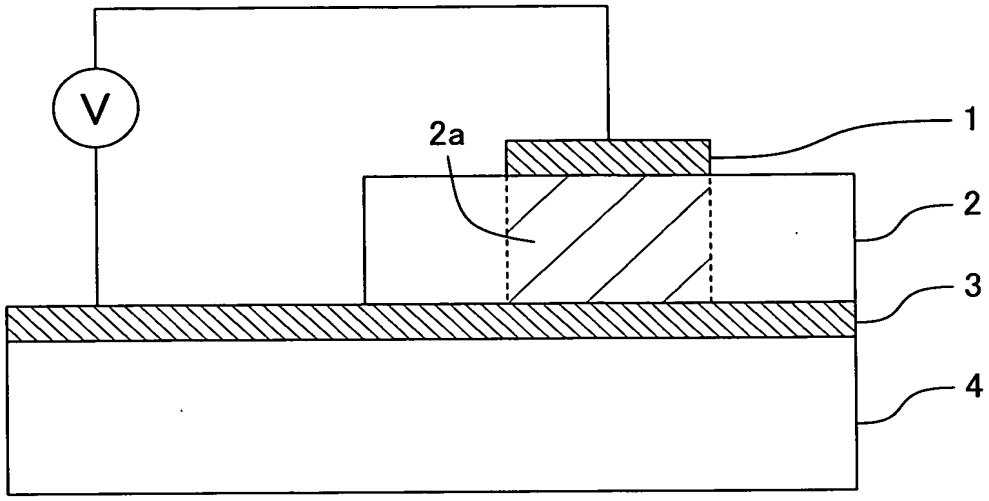
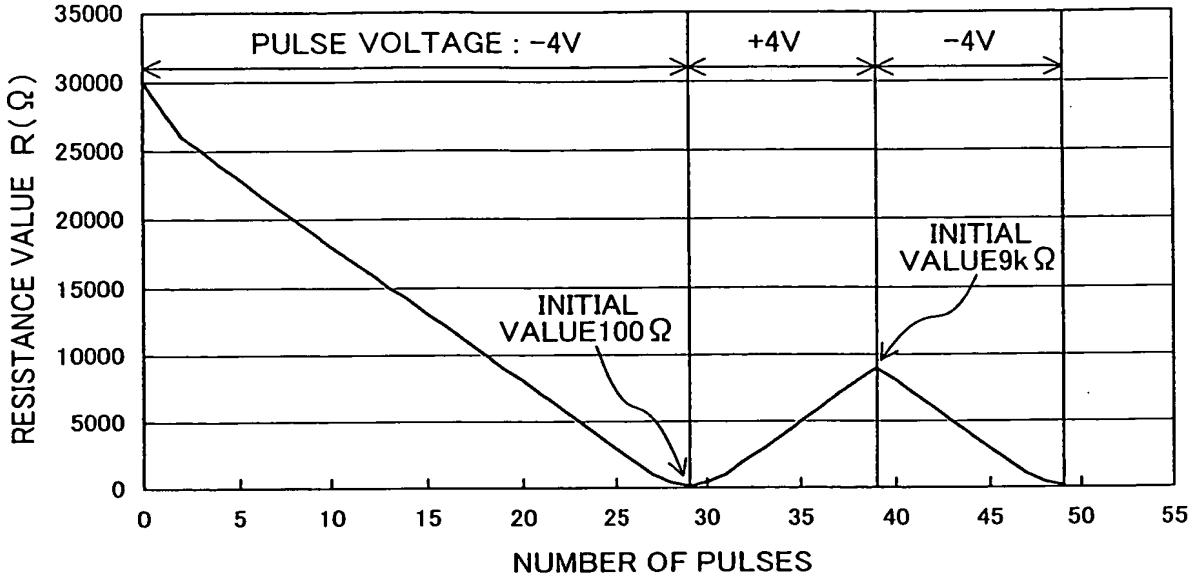


FIG. 2

(a) VARIABLE RESISTOR α



(b) VARIABLE RESISTOR β

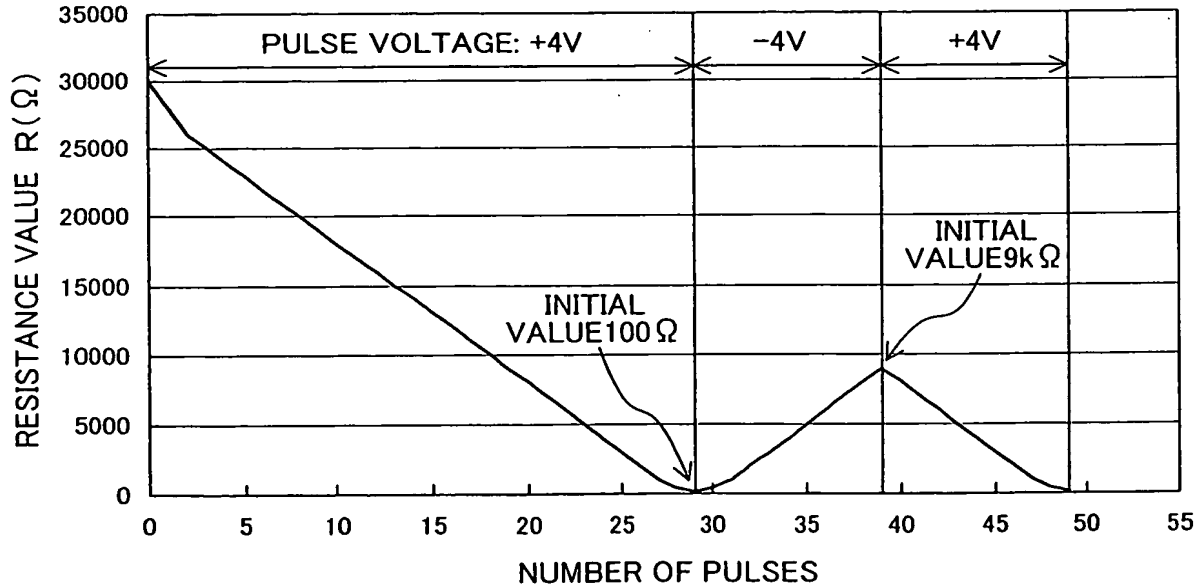
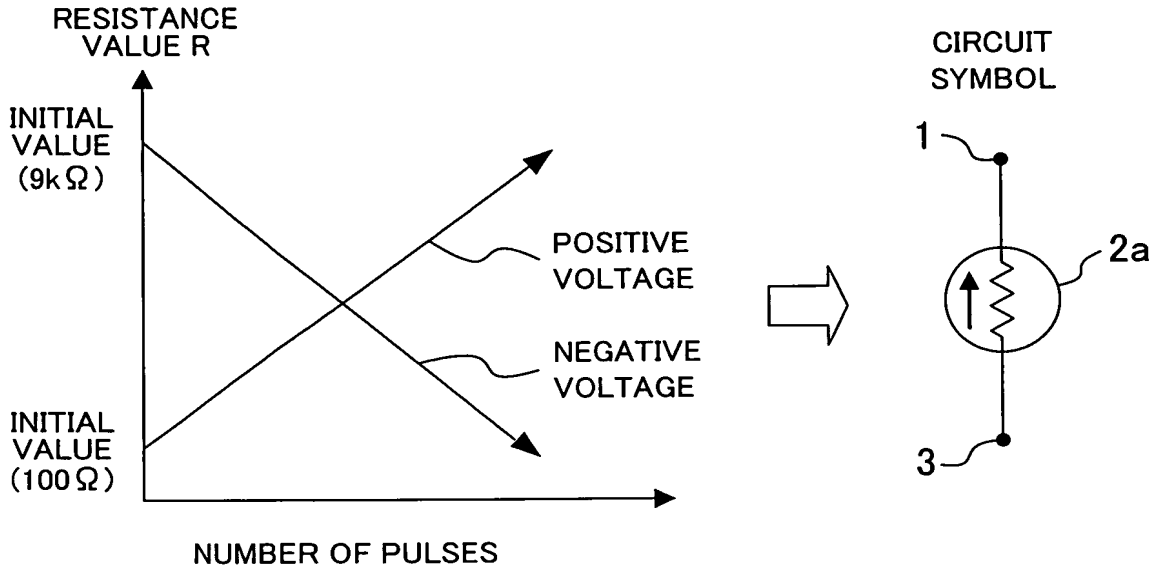


FIG. 3

(a) VARIABLE RESISTOR α



(b) VARIABLE RESISTOR β

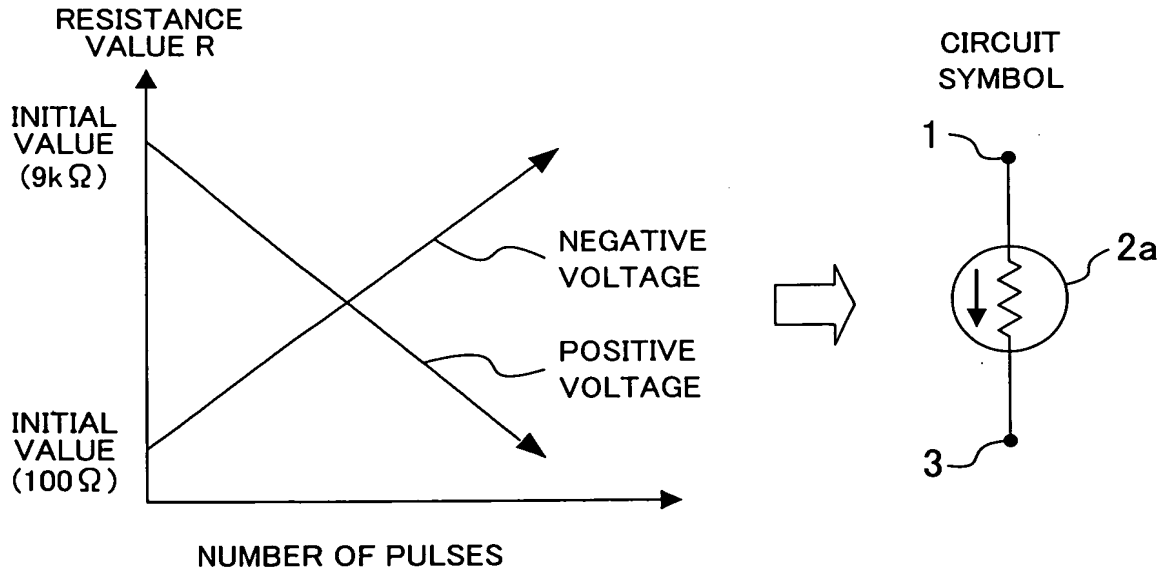
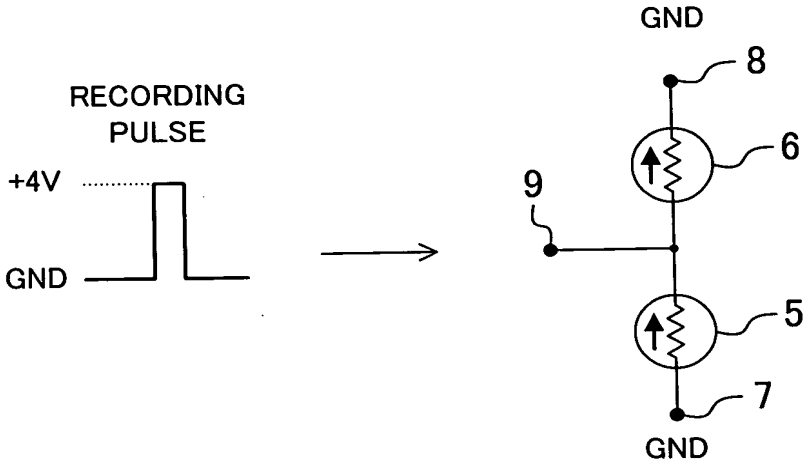
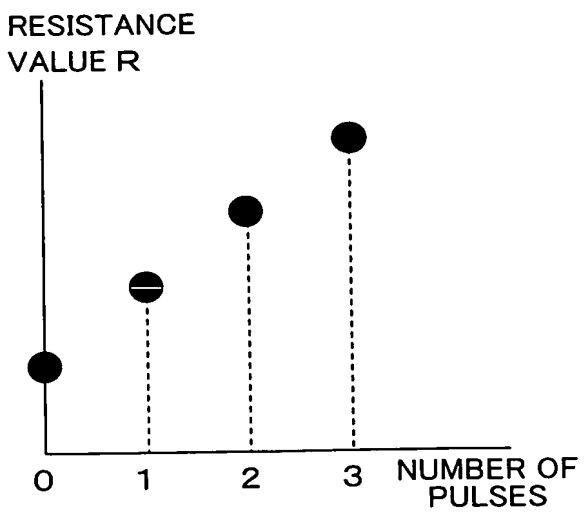


FIG. 4

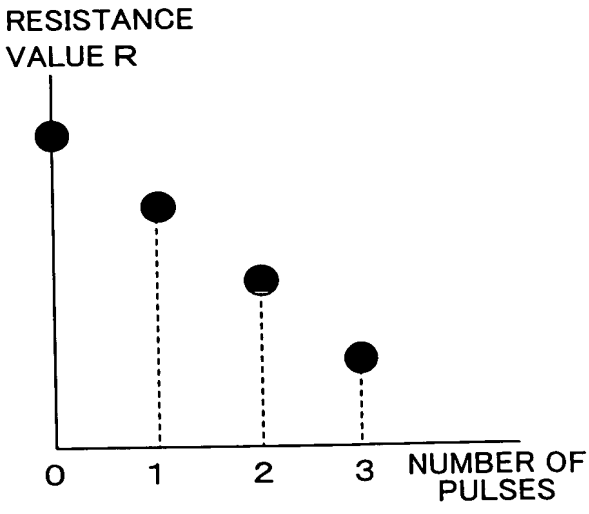
(a) RECORDING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR



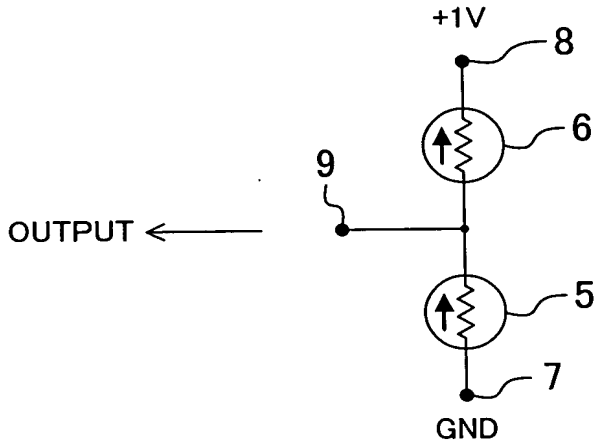
<RESISTANCE CHANGE OF VARIABLE RESISTOR 5>



<RESISTANCE CHANGE OF VARIABLE RESISTOR 6>

FIG. 5

(a) REPRODUCTION



(b) REPRODUCTION OUTPUT VOLTAGE

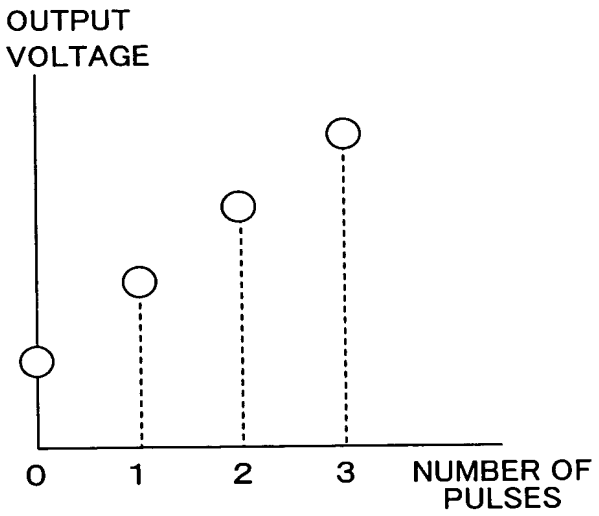
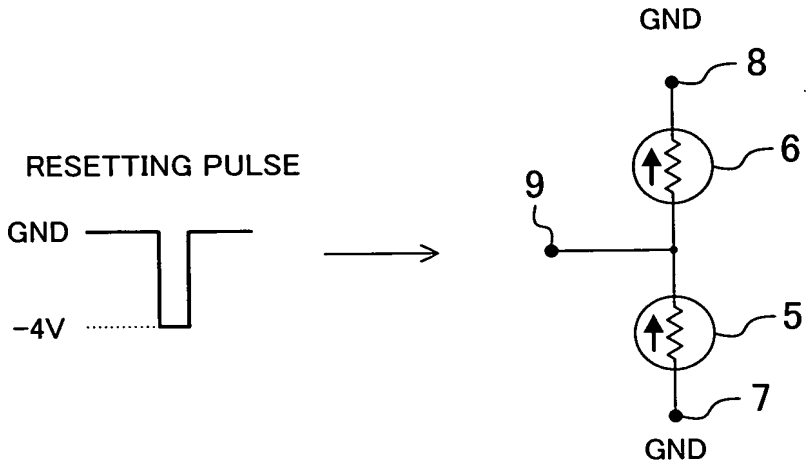
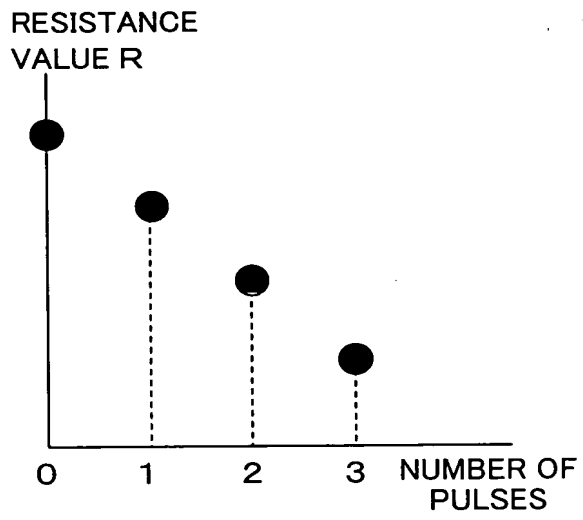


FIG. 6

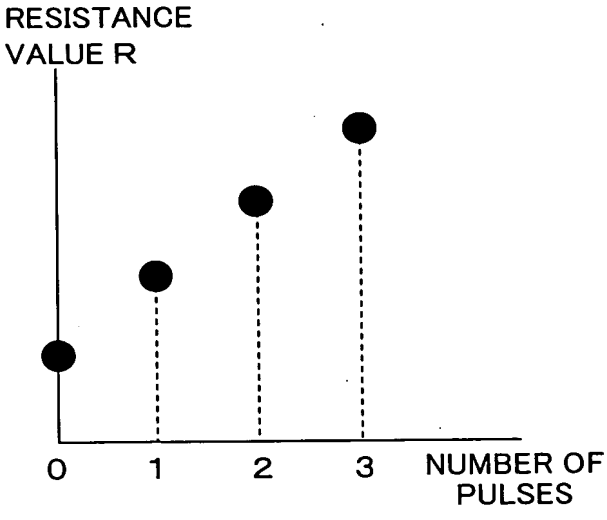
(a) RESETTING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR



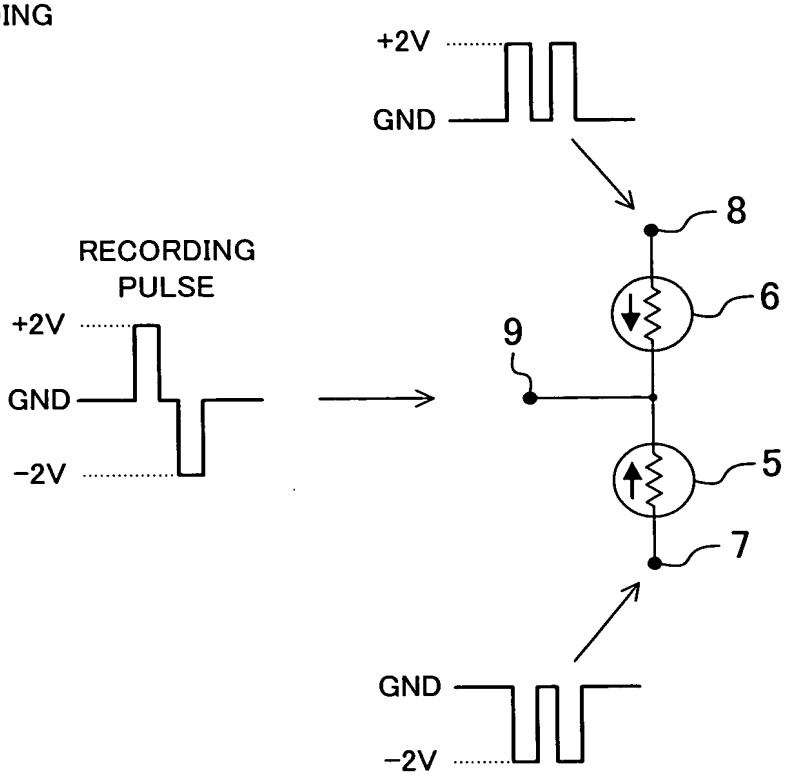
<RESISTANCE CHANGE OF VARIABLE RESISTOR 5>



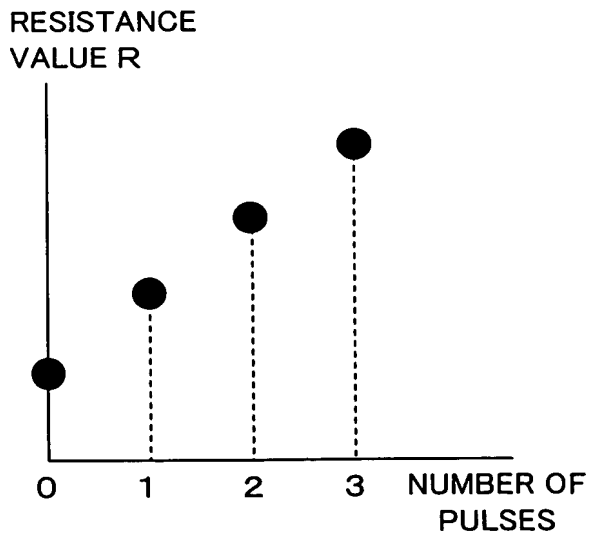
<RESISTANCE CHANGE OF VARIABLE RESISTOR 6>

FIG. 7

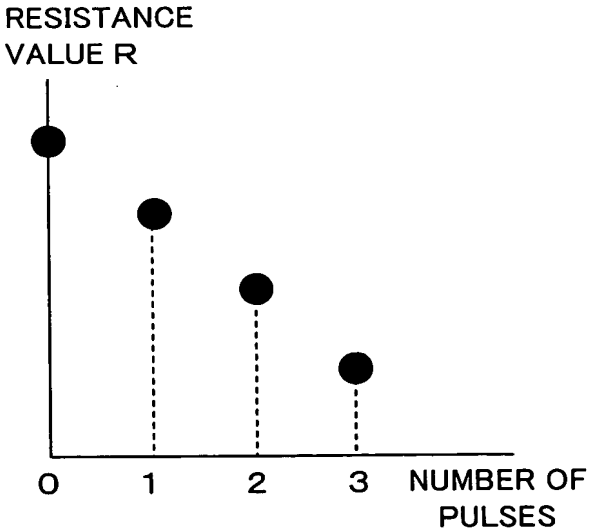
(a) RECORDING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR



<RESISTANCE CHANGE OF VARIABLE RESISTOR 5>



<RESISTANCE CHANGE OF VARIABLE RESISTOR 6>

FIG. 8

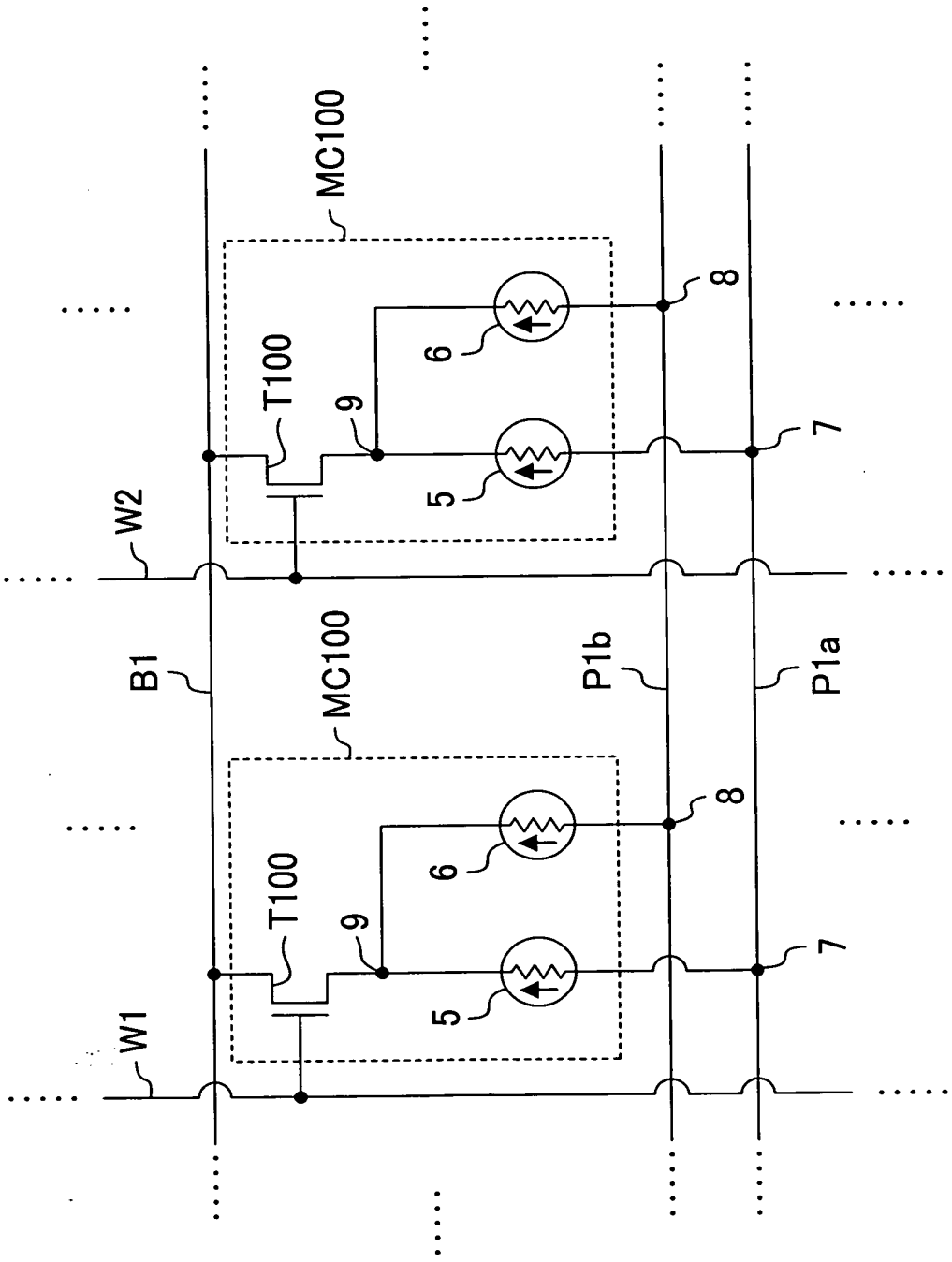


FIG. 9

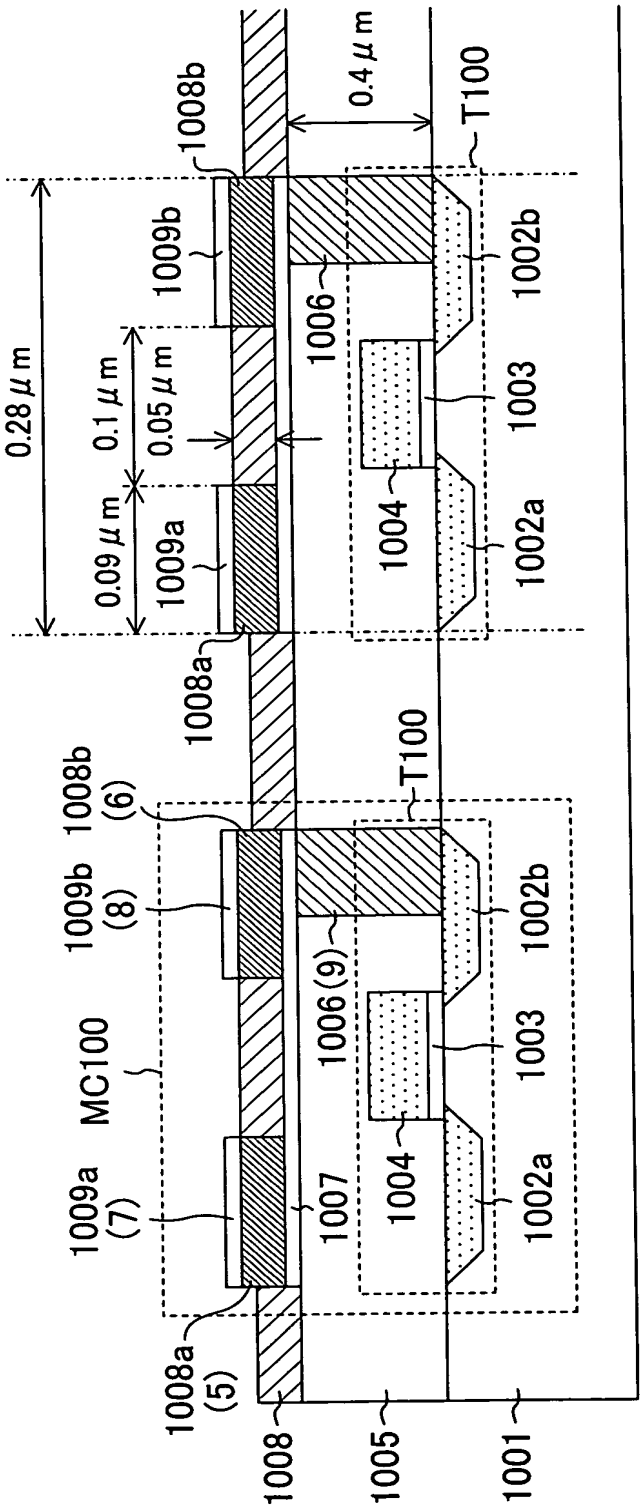
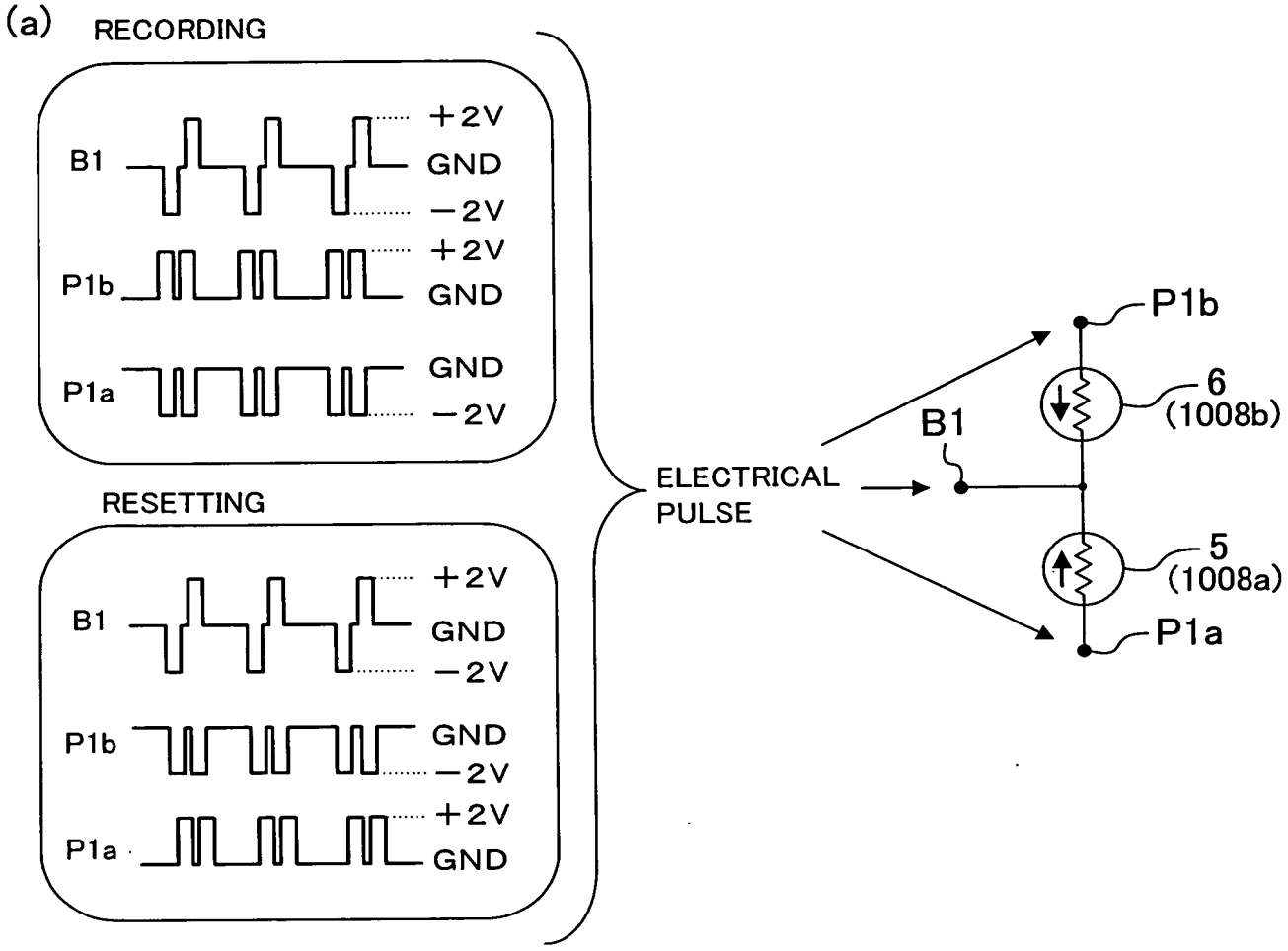

0.28μm
0.1μm
0.05μm
0.09μm
0.4μm
1008b
1009b
1009a
1008a
1006
1004
1003
1002b
1002a
T100
MC100
(5)
(6)
(7)
(8)
(9)
1007
1008
1005
1001

FIG. 10


(a)
RECORDING
B1
+2V
GND
−2V
P1b
+2V
GND
P1a
GND
−2V
RESETTING
B1
+2V
GND
−2V
P1b
GND
−2V
P1a
+2V
GND
ELECTRICAL PULSE
B1
P1b
6
(1008b)
5
(1008a)
P1a

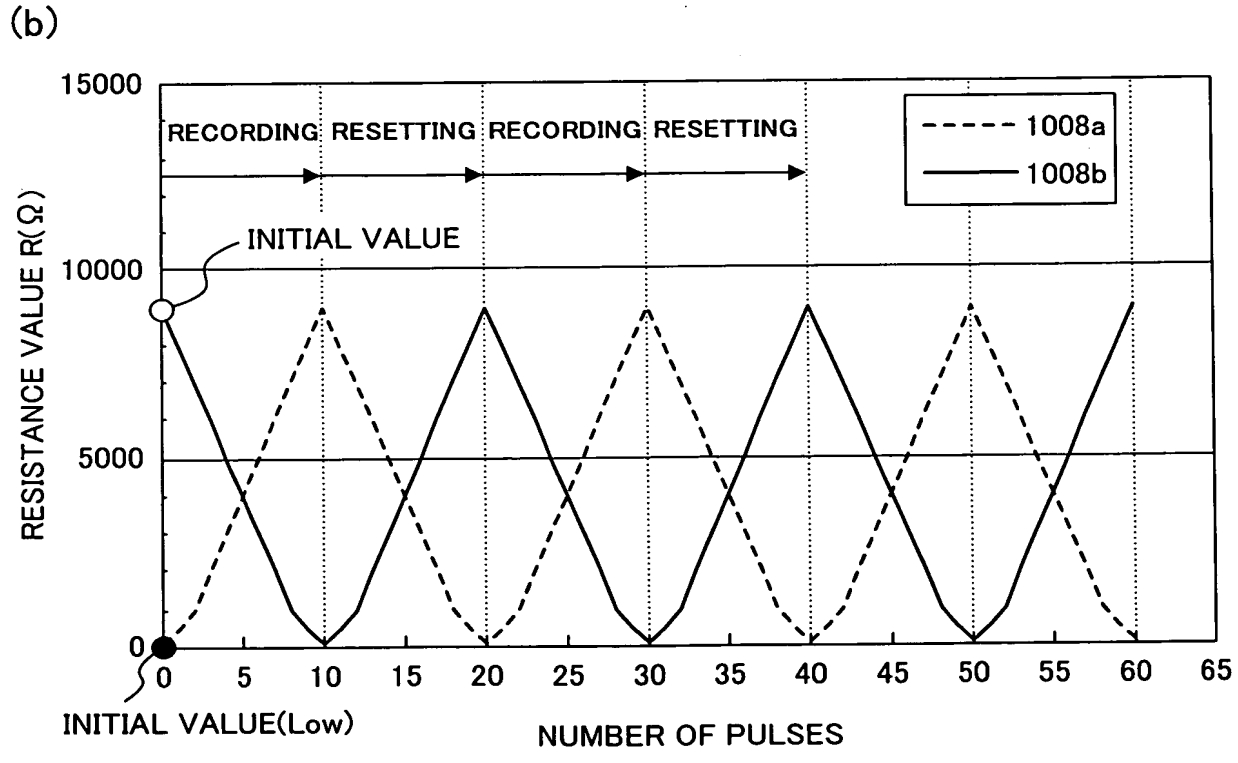
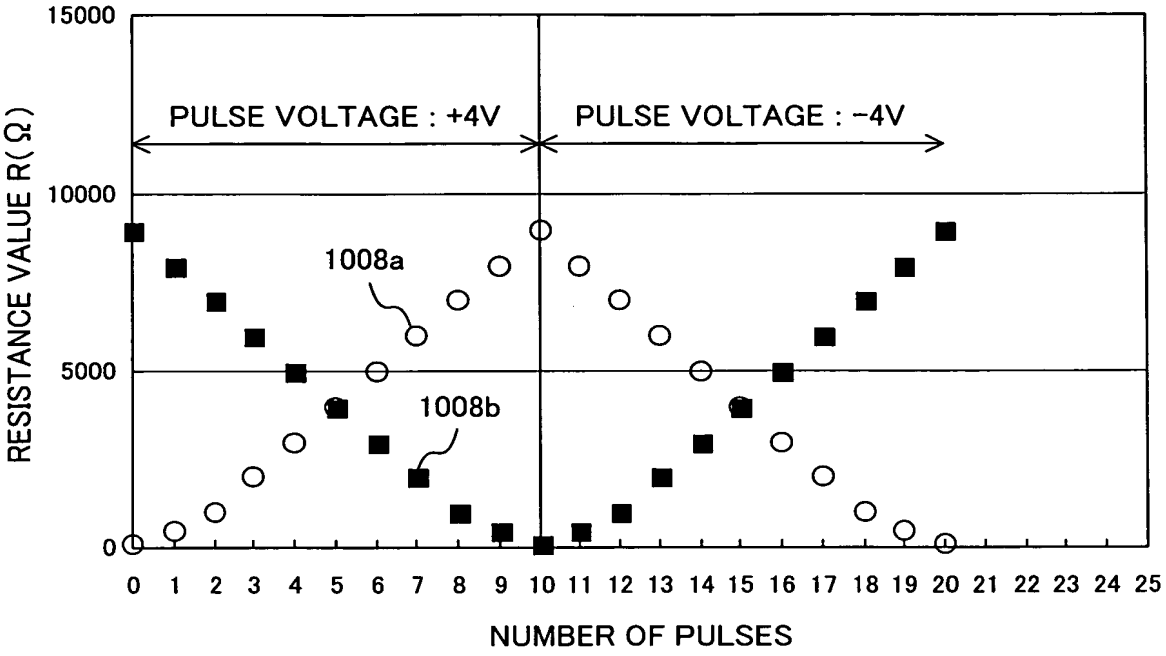

(b)
15000
10000
5000
0
RESISTANCE VALUE R(Ω)
RECORDING
RESETTING
RECORDING
RESETTING
1008a
1008b
INITIAL VALUE
INITIAL VALUE(Low)
0
5
10
15
20
25
30
35
40
45
50
55
60
65
NUMBER OF PULSES

FIG. 11

(a) RESISTANCE CHANGE WITH NUMBER OF PULSES



(b) OUTPUT VOLTAGE IN READOUT OF RECORDING STATE

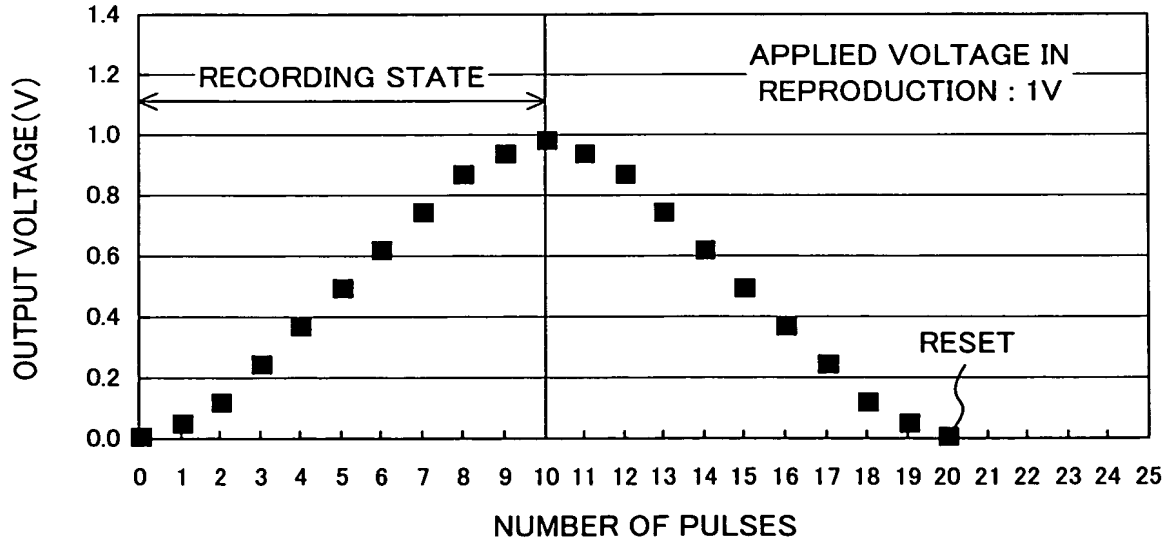
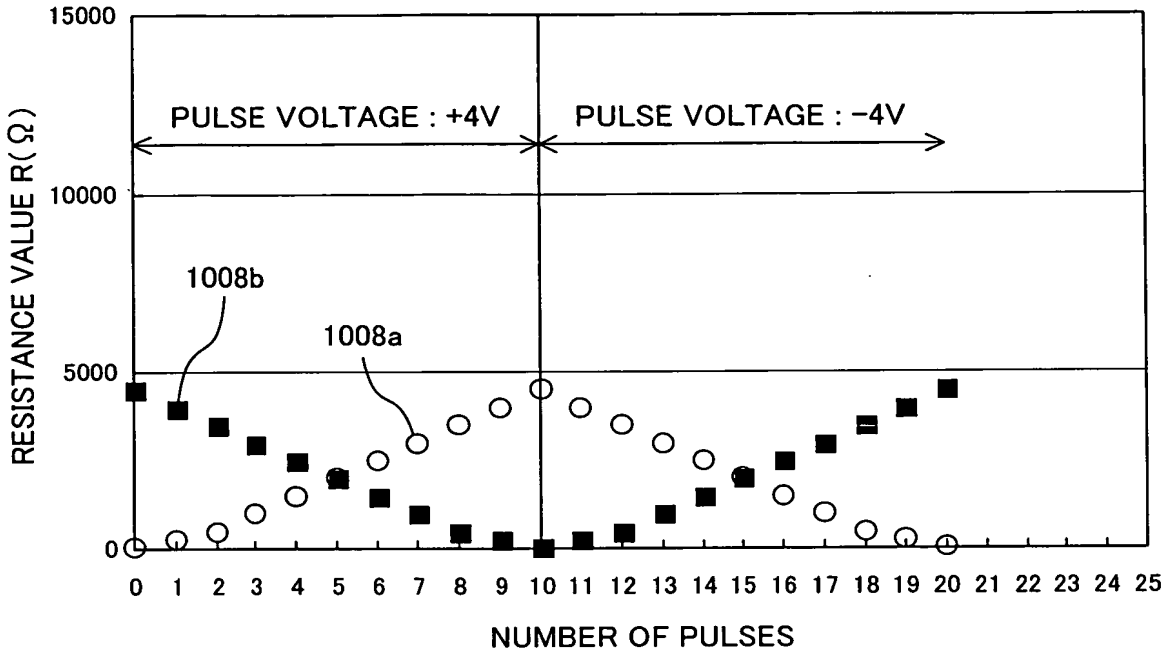


FIG. 12

(a) RESISTANCE CHANGE WITH NUMBER OF PULSES



(b) OUTPUT VOLTAGE IN READOUT OF RECORDING STATE

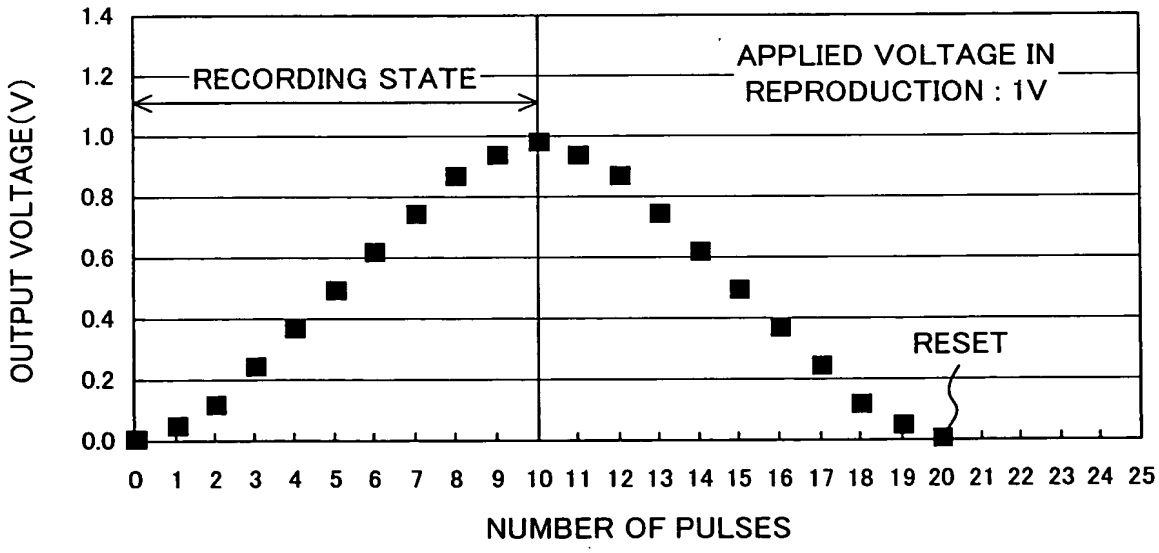


FIG. 13

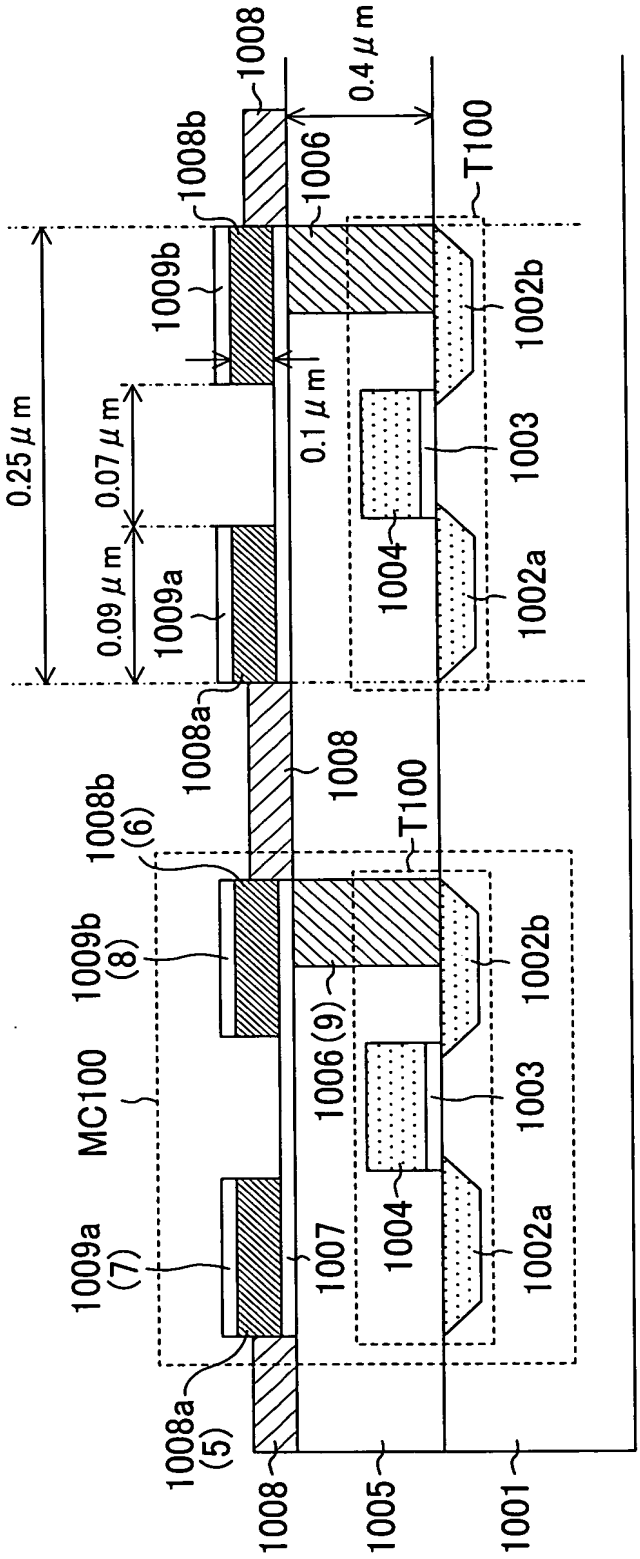

1008
0.4 μm
1008b
1006
T100
1009b
1002b
0.25 μm
0.07 μm
0.1 μm
1003
0.09 μm
1009a
1004
1002a
1008a
1008
1008b
(6)
T100
1009b
(8)
1002b
MC100
1006 (9)
1003
1009a
(7)
1007
1004
1002a
1008a
(5)
1008
1005
1001

FIG. 14

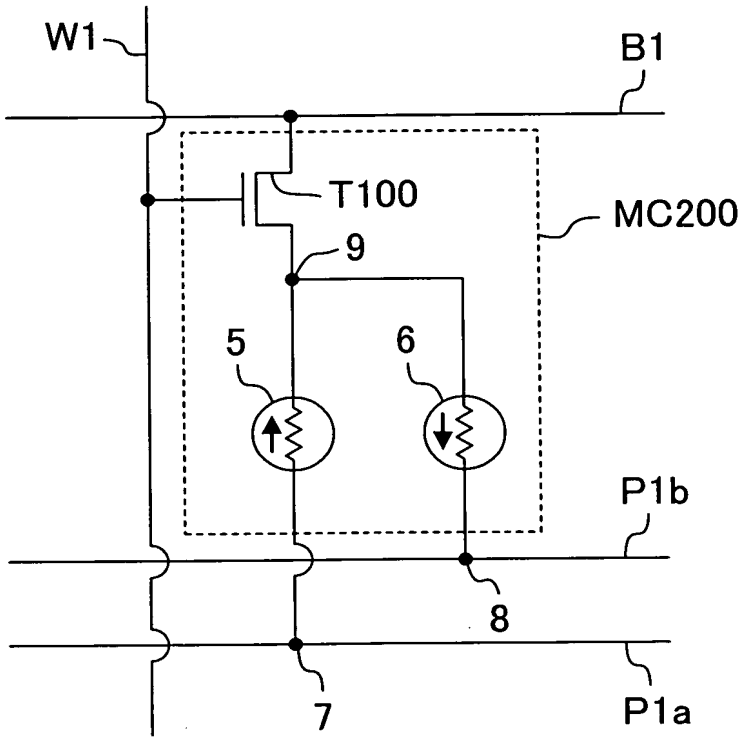
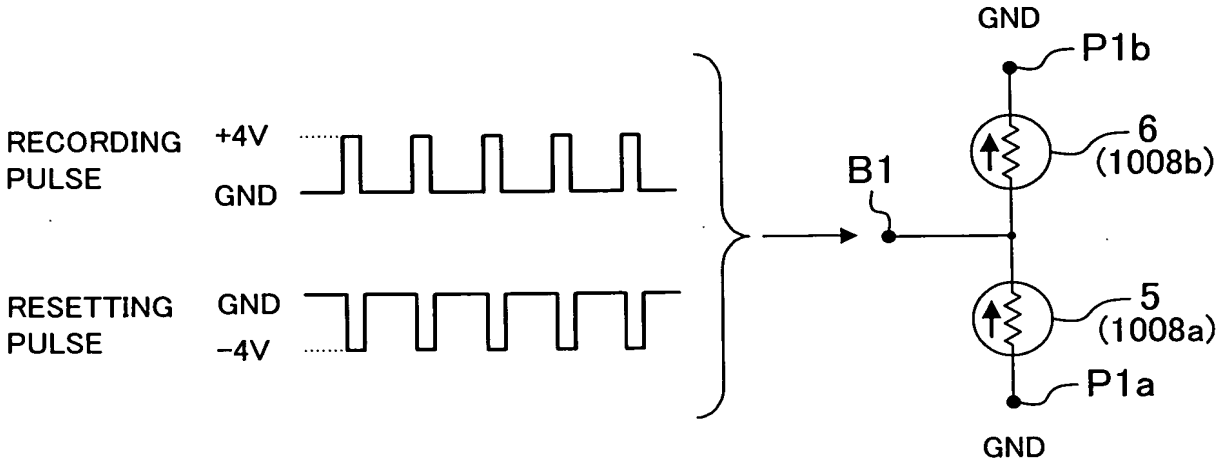
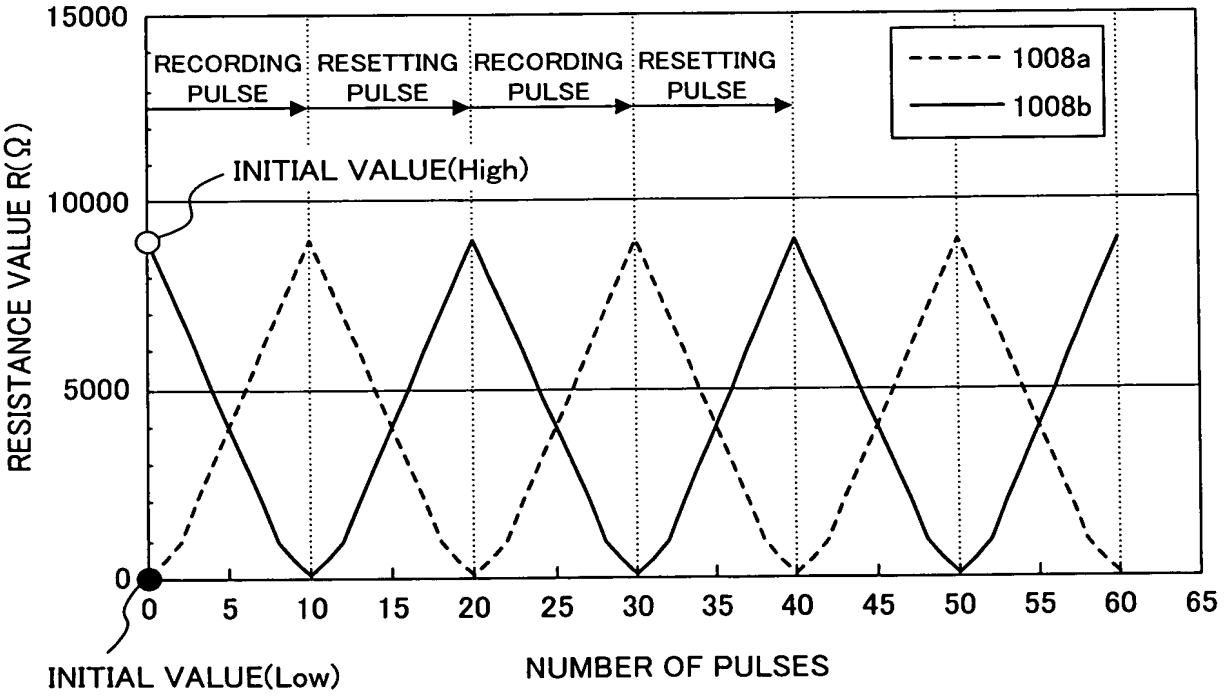


FIG. 15

(a)


RECORDING PULSE
+4V
GND
RESETTING PULSE
GND
-4V
B1
GND
P1b
6
(1008b)
5
(1008a)
P1a
GND

(b)


15000
10000
5000
0
RESISTANCE VALUE R(Ω)
RECORDING PULSE
RESETTING PULSE
RECORDING PULSE
RESETTING PULSE
1008a
1008b
INITIAL VALUE(High)
INITIAL VALUE(Low)
0
5
10
15
20
25
30
35
40
45
50
55
60
65
NUMBER OF PULSES

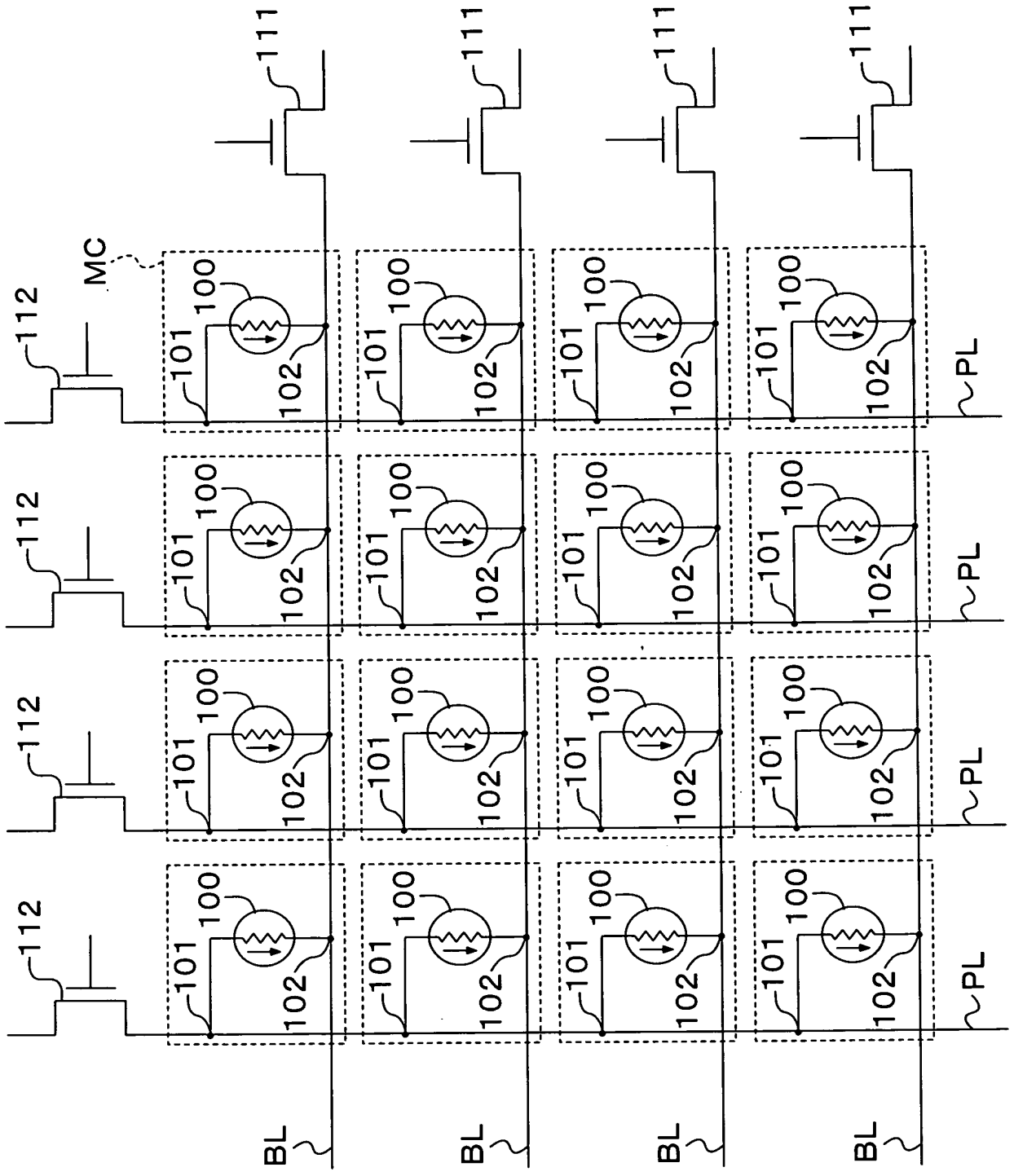


FIG. 16

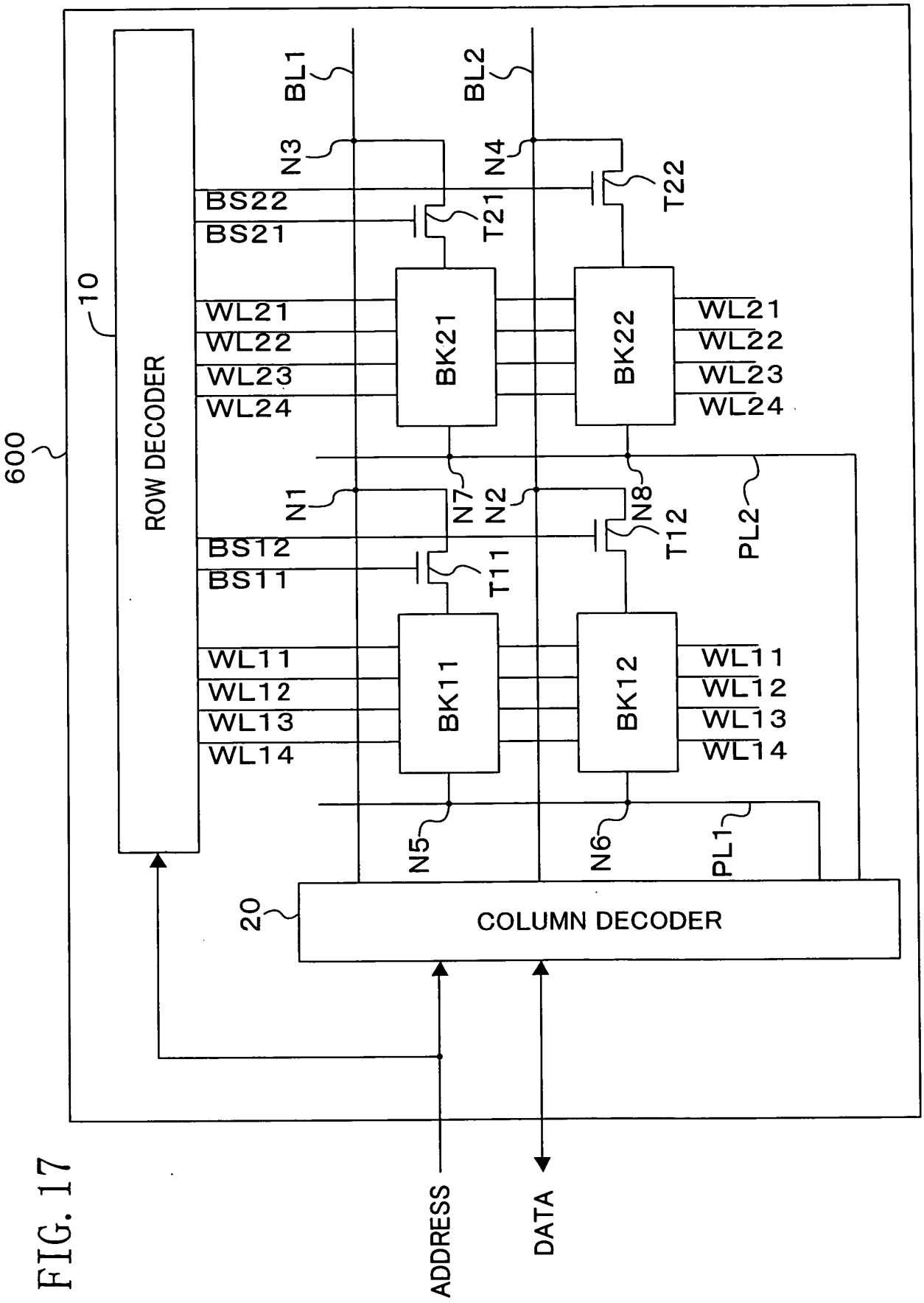

600
10
ROW DECODER
BL1
BL2
N3
N4
T22
BS22
BS21
T21
WL21
WL22
WL23
WL24
BK21
BK22
WL21
WL22
WL23
WL24
N1
N7
N2
N8
T12
PL2
BS12
BS11
T11
WL11
WL12
WL13
WL14
BK11
BK12
WL11
WL12
WL13
WL14
N5
N6
PL1
20
COLUMN DECODER
ADDRESS
DATA

FIG. 17

FIG. 18

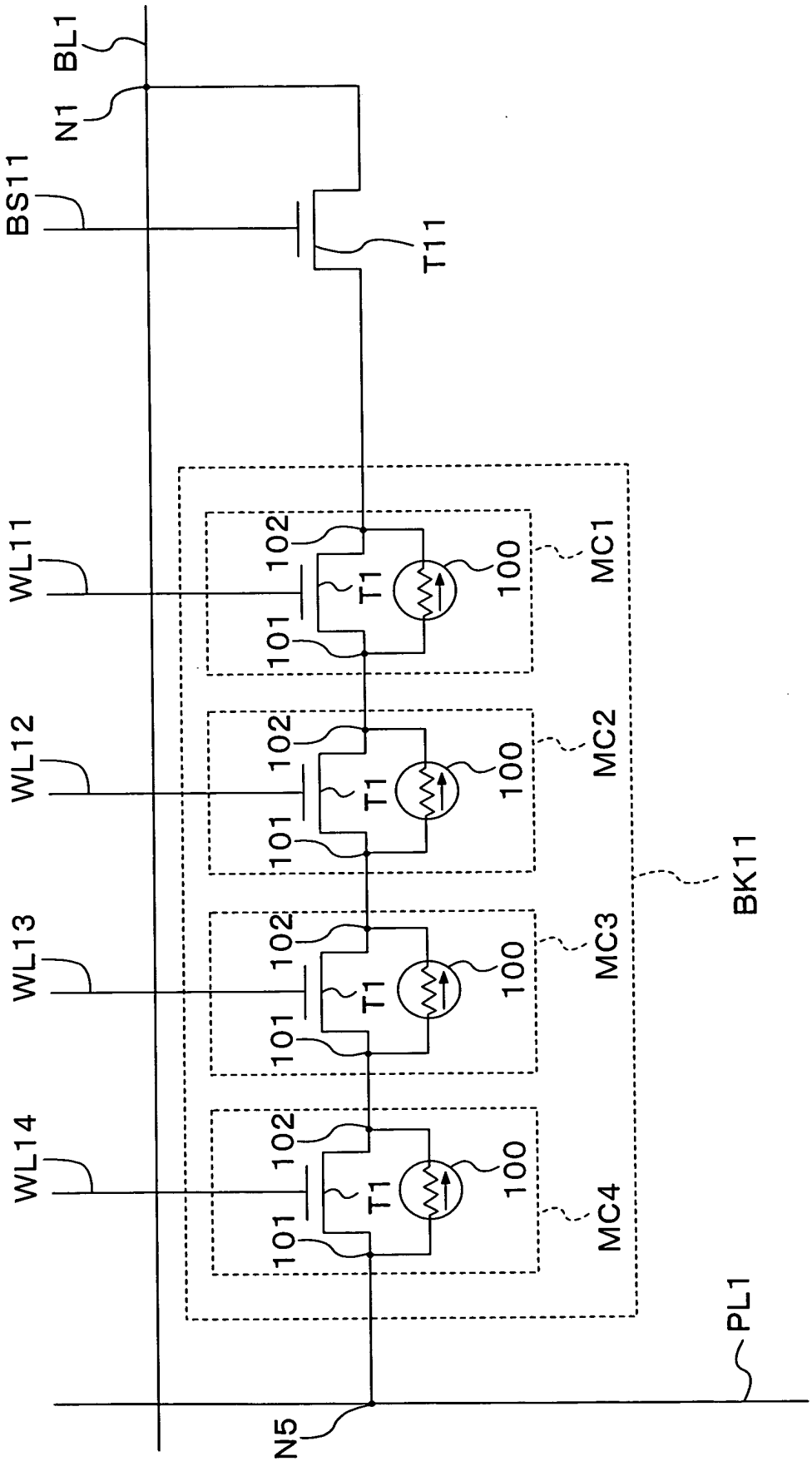
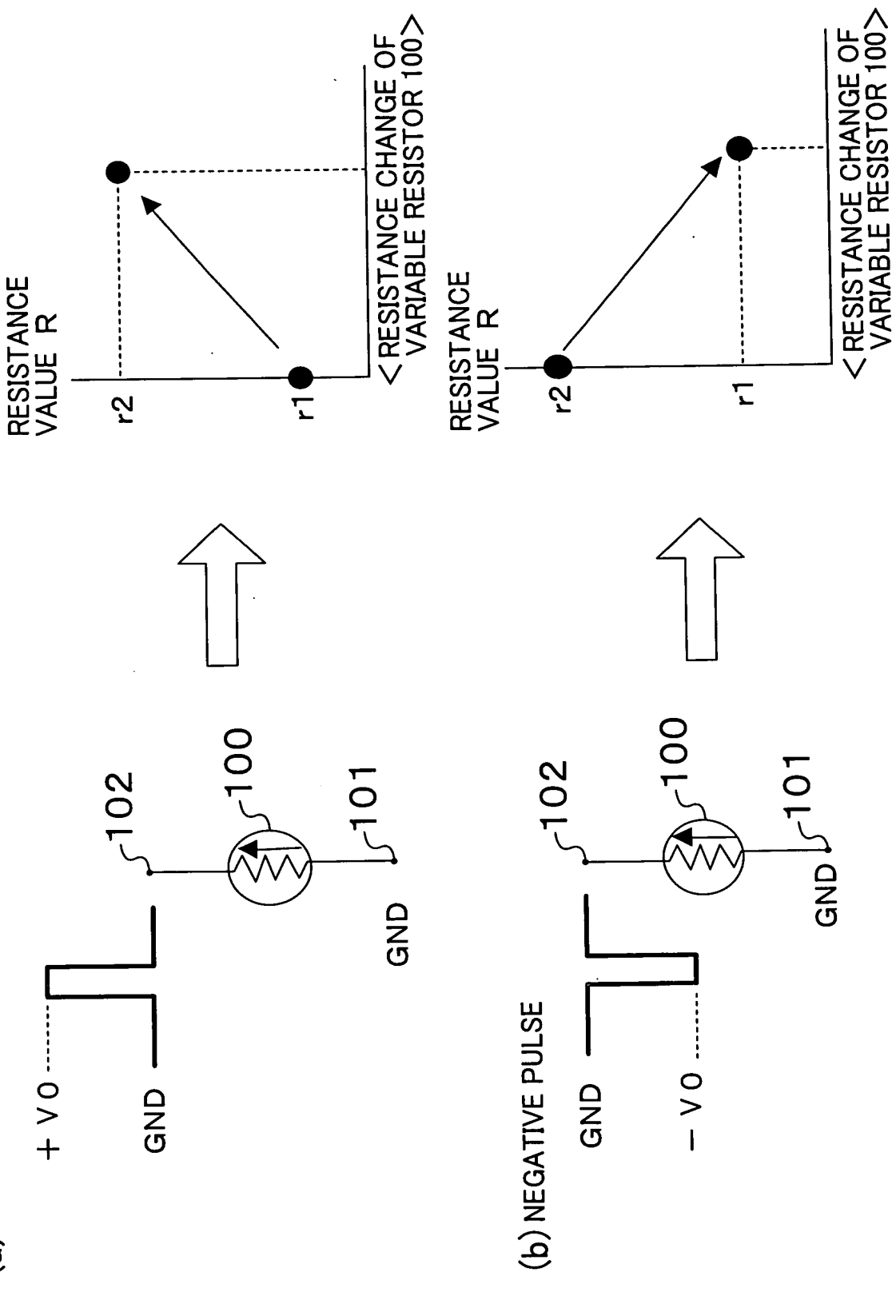

BL1
N1
BS11
T11
WL11
WL12
WL13
WL14
102
101
T1
100
MC1
MC2
MC3
MC4
BK11
N5
PL1

FIG. 19


(a) POSITIVE PULSE
+ V 0
GND
102
100
101
GND
RESISTANCE VALUE R
r2
r1
< RESISTANCE CHANGE OF VARIABLE RESISTOR 100 >
(b) NEGATIVE PULSE
GND
− V 0
102
100
101
GND
RESISTANCE VALUE R
r2
r1
< RESISTANCE CHANGE OF VARIABLE RESISTOR 100 >

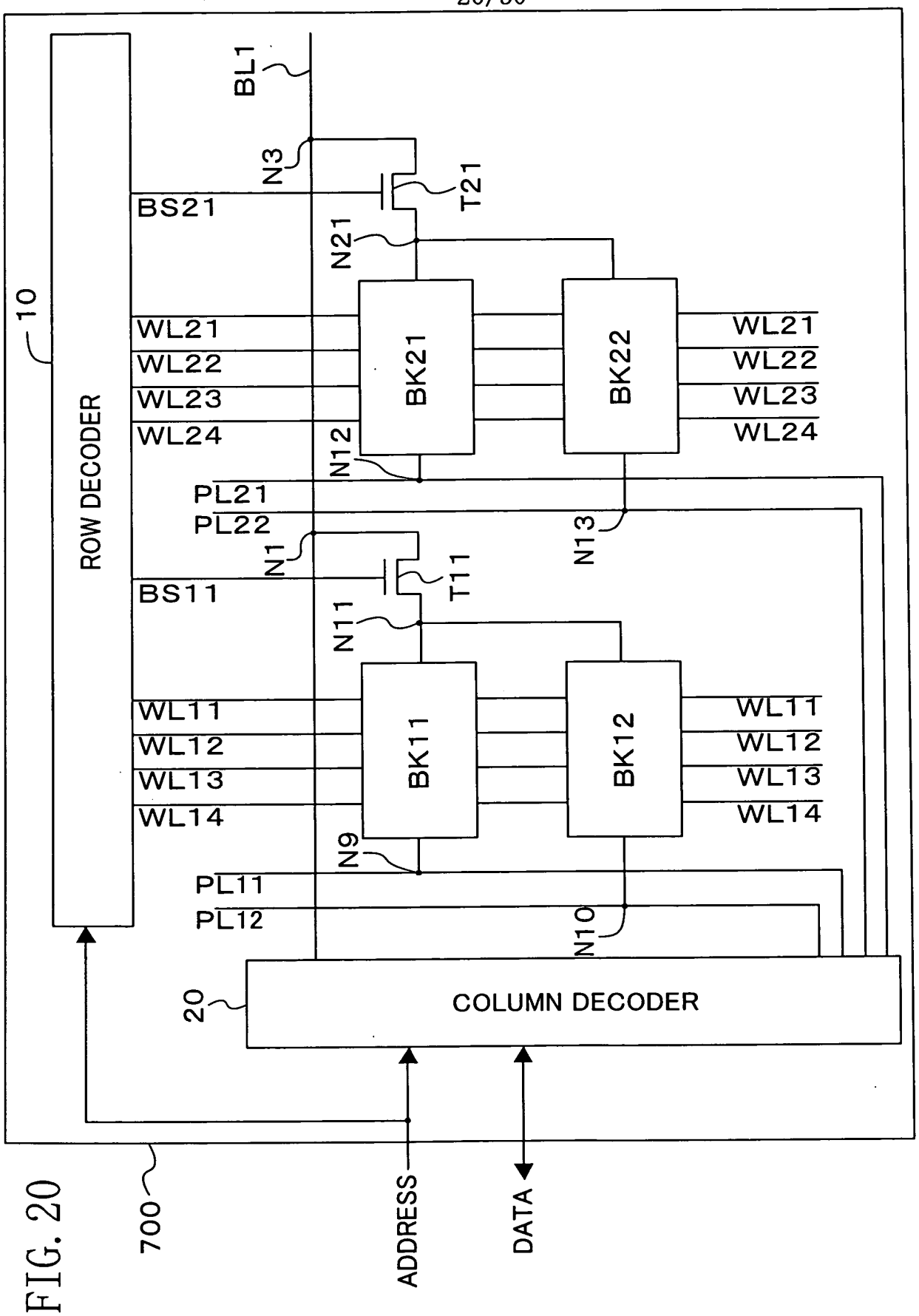

BL1
N3
T21
BS21
N21
10
WL21
WL22
WL23
WL24
BK21
BK22
WL21
WL22
WL23
WL24
N12
PL21
PL22
N13
N1
T11
BS11
N11
ROW DECODER
WL11
WL12
WL13
WL14
BK11
BK12
WL11
WL12
WL13
WL14
N9
PL11
PL12
N10
20
COLUMN DECODER
700
ADDRESS
DATA

FIG. 20

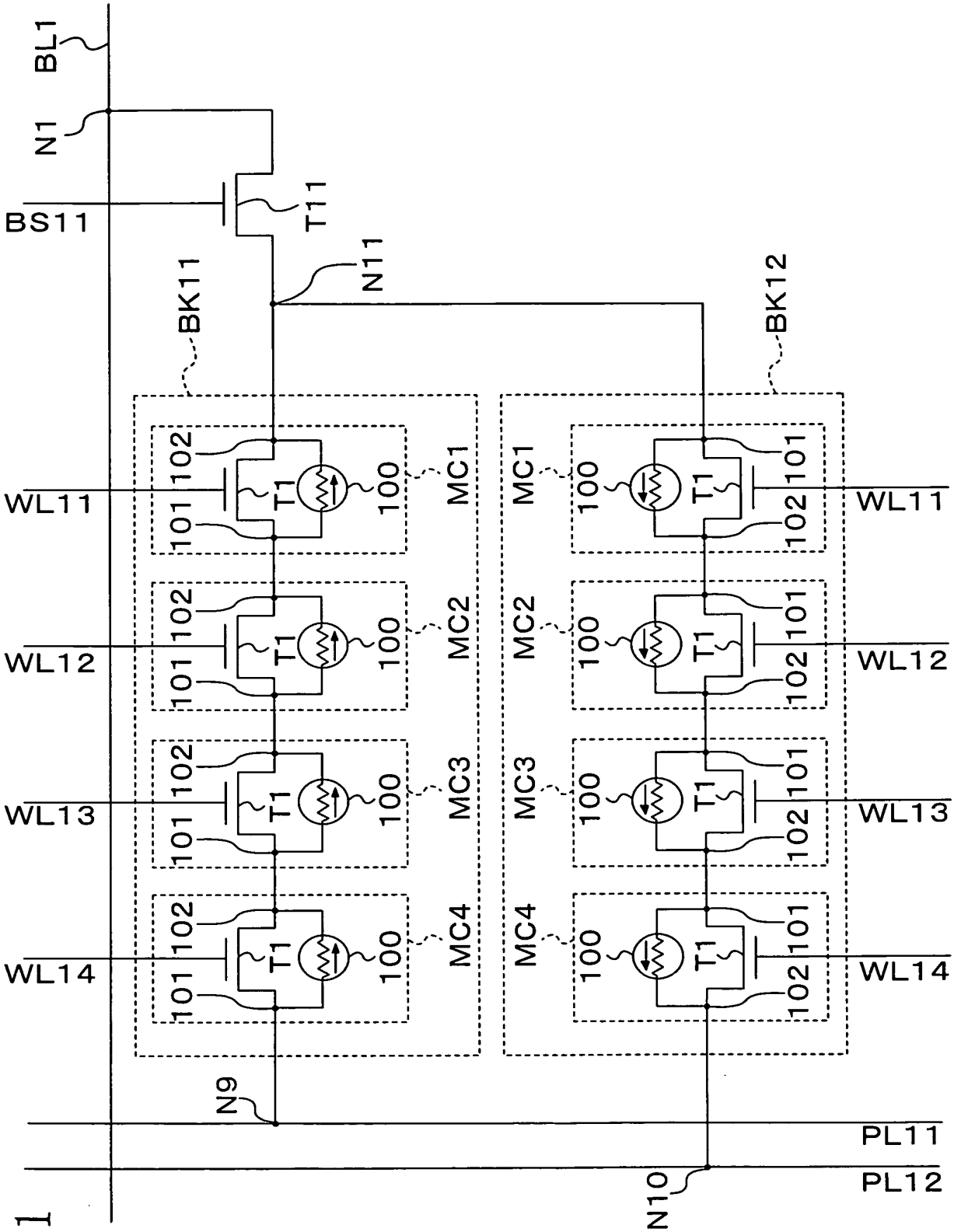

BL1
N1
BS11
T11
N11
BK11
BK12
WL11
WL12
WL13
WL14
MC1
MC2
MC3
MC4
T1
100
101
102
N9
N10
PL11
PL12

FIG. 21

FIG. 22

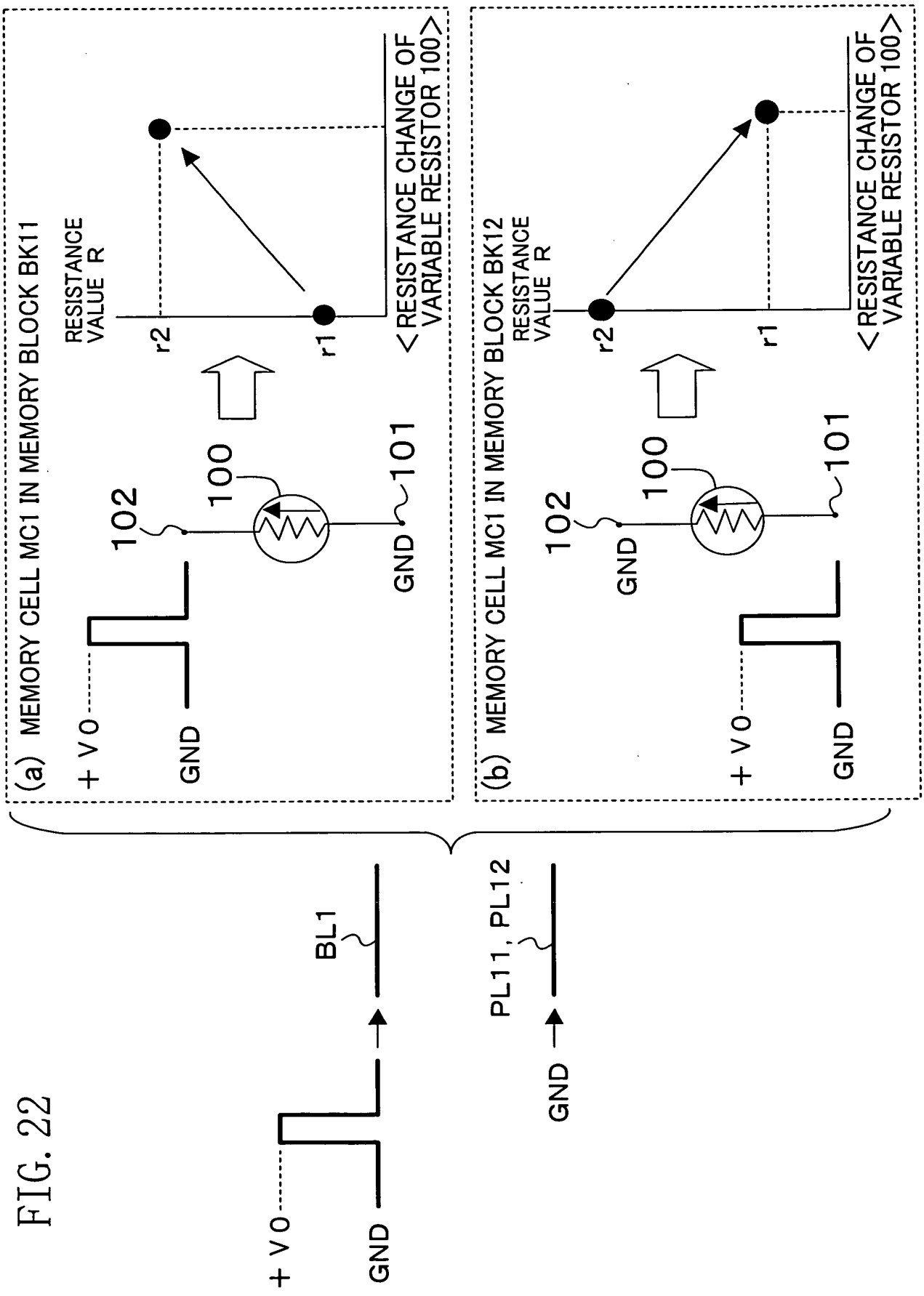

(a) MEMORY CELL MC1 IN MEMORY BLOCK BK11
RESISTANCE VALUE R
r2
r1
< RESISTANCE CHANGE OF VARIABLE RESISTOR 100>
102
100
101
GND
+ V0
GND
(b) MEMORY CELL MC1 IN MEMORY BLOCK BK12
RESISTANCE VALUE R
r2
r1
< RESISTANCE CHANGE OF VARIABLE RESISTOR 100>
102
100
101
GND
+ V0
GND
BL1
+ V0
GND
PL11, PL12
GND

FIG. 23

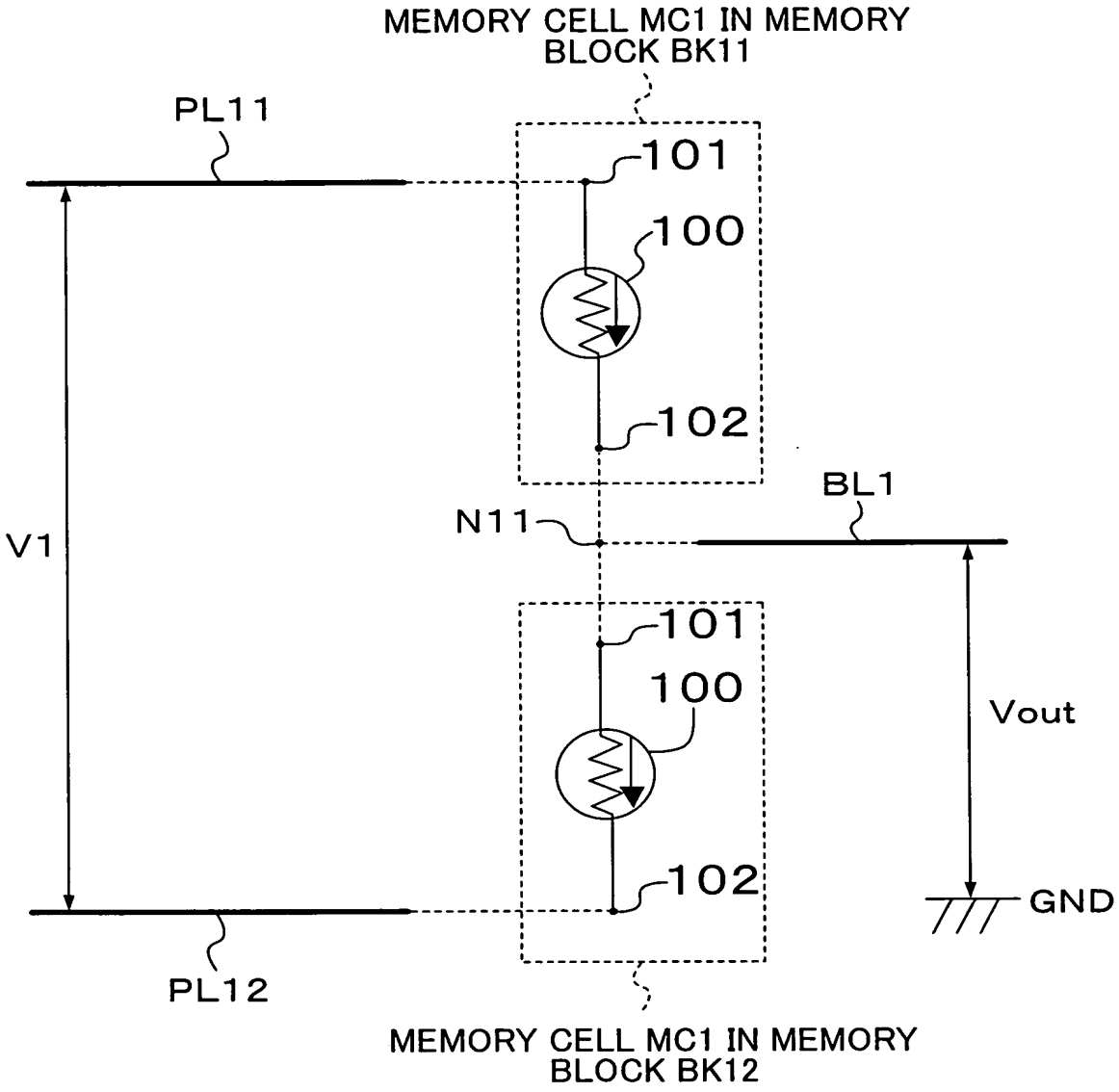
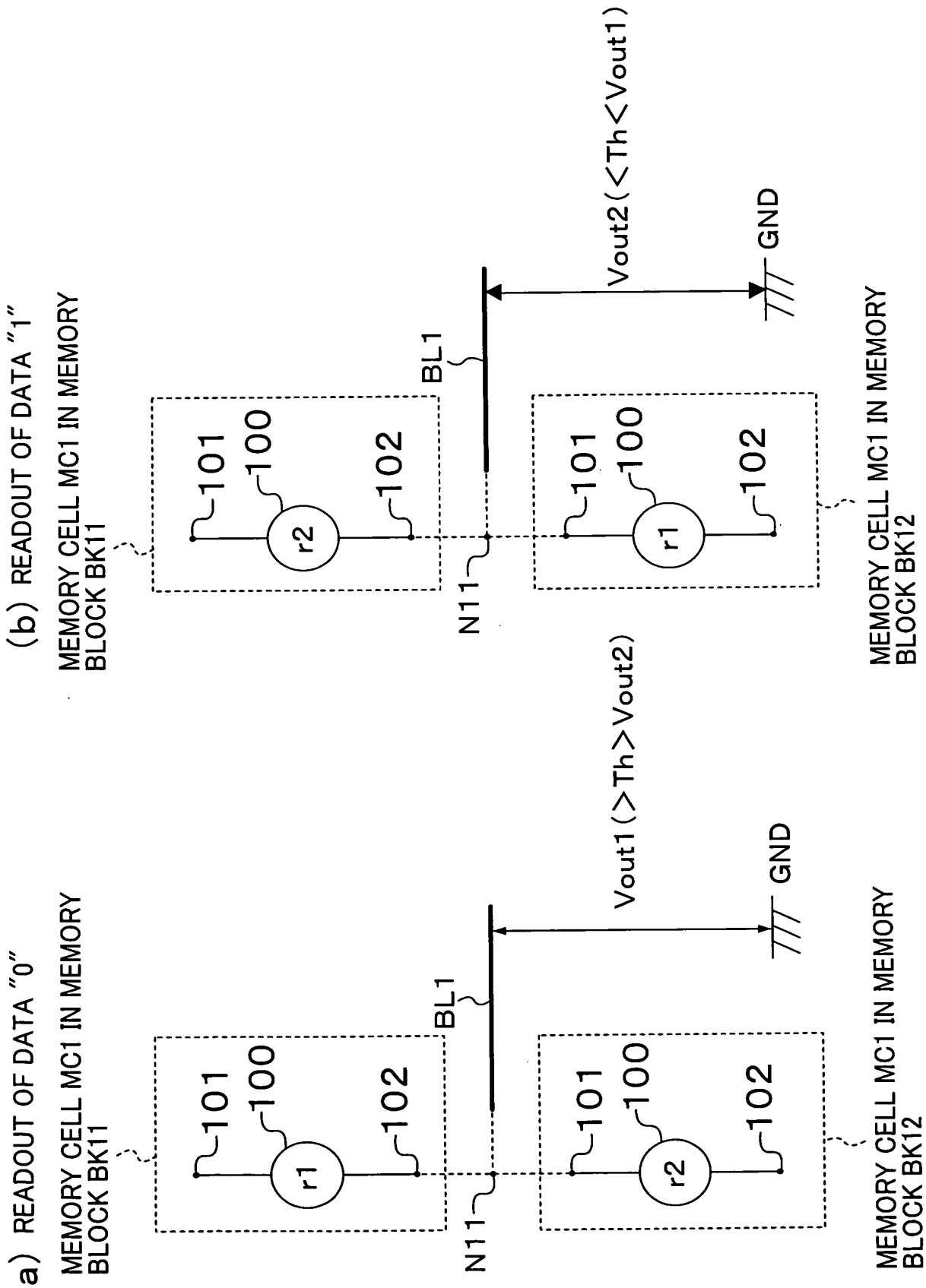

MEMORY CELL MC1 IN MEMORY BLOCK BK11
PL11
101
100
102
BL1
N11
V1
101
100
Vout
102
GND
PL12
MEMORY CELL MC1 IN MEMORY BLOCK BK12

FIG. 24


(a) READOUT OF DATA "0"
MEMORY CELL MC1 IN MEMORY BLOCK BK11
101
100
r1
102
BL1
N11
Vout1 (>Th>Vout2)
GND
MEMORY CELL MC1 IN MEMORY BLOCK BK12
101
100
r2
102
(b) READOUT OF DATA "1"
MEMORY CELL MC1 IN MEMORY BLOCK BK11
101
100
r2
102
BL1
N11
Vout2 (<Th<Vout1)
GND
MEMORY CELL MC1 IN MEMORY BLOCK BK12
101
100
r1
102

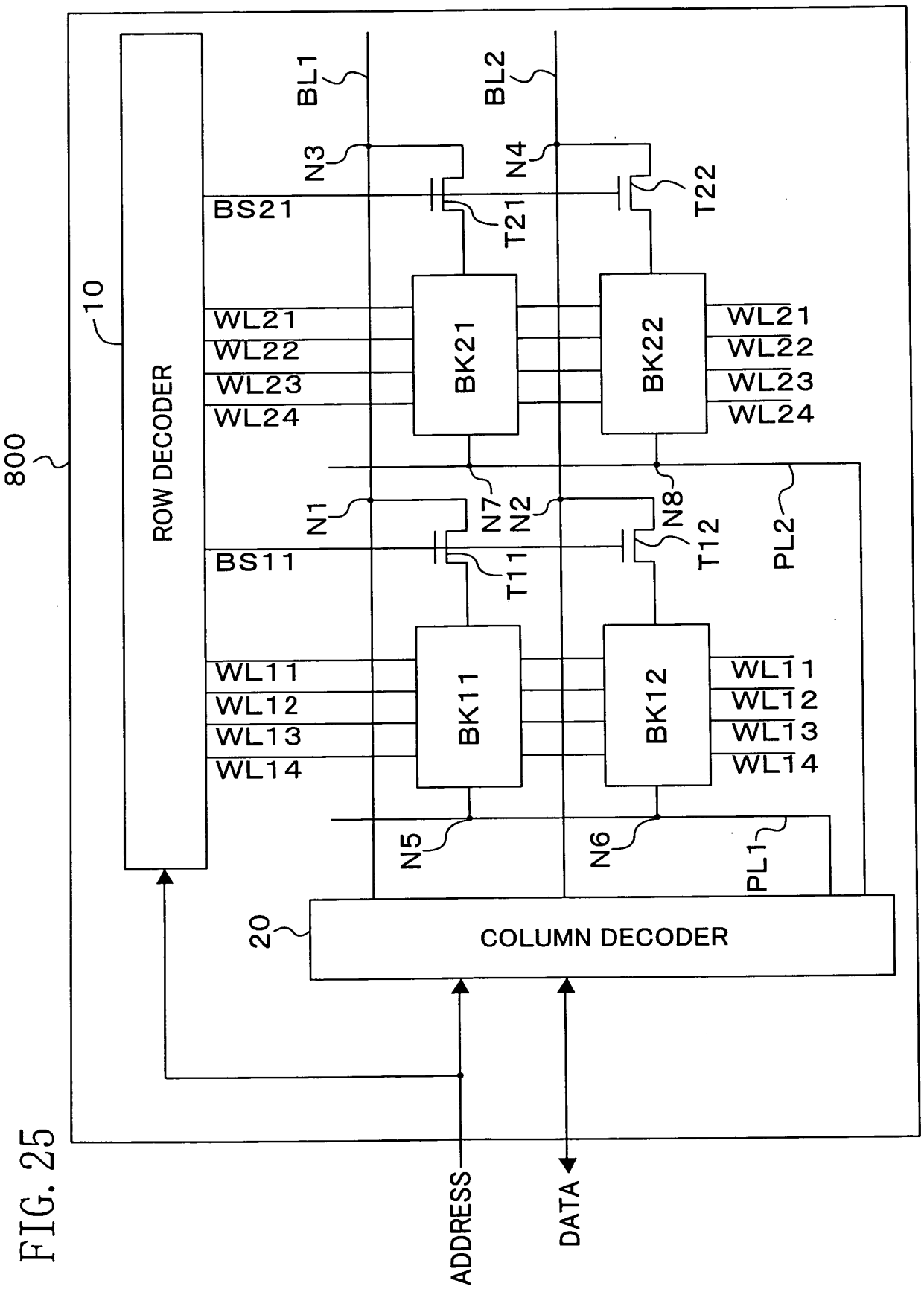

800
10
ROW DECODER
BL1
BL2
N3
N4
T22
BS21
T21
WL21
WL22
WL23
WL24
BK21
BK22
WL21
WL22
WL23
WL24
N1
N7
N2
N8
PL2
T12
BS11
T11
WL11
WL12
WL13
WL14
BK11
BK12
WL11
WL12
WL13
WL14
N5
N6
PL1
20
COLUMN DECODER
ADDRESS
DATA

FIG. 25

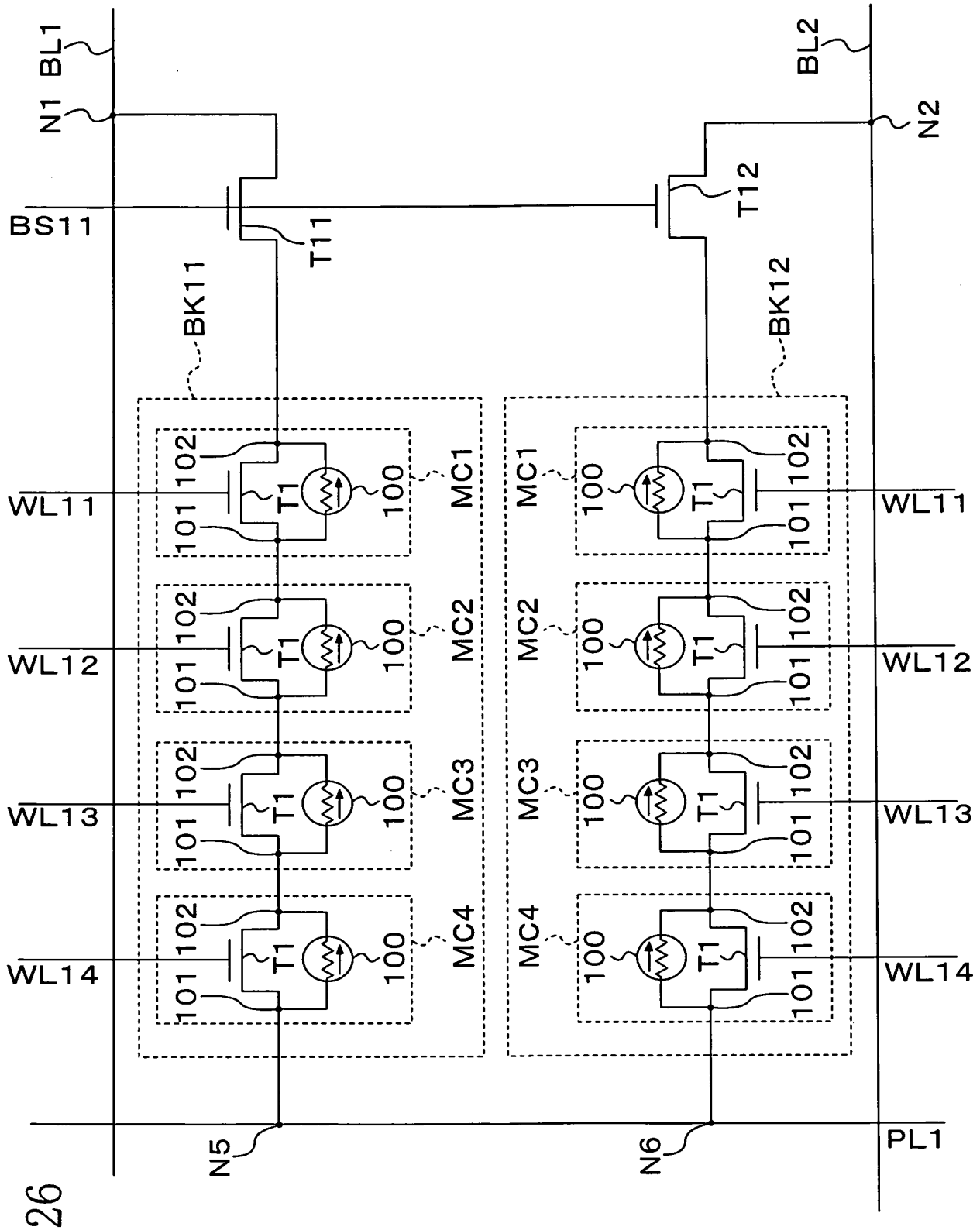

BL1
N1
BL2
N2
BS11
T11
T12
BK11
BK12
WL11
WL12
WL13
WL14
MC1
MC2
MC3
MC4
T1
100
101
102
N5
N6
PL1

FIG. 26

FIG. 27

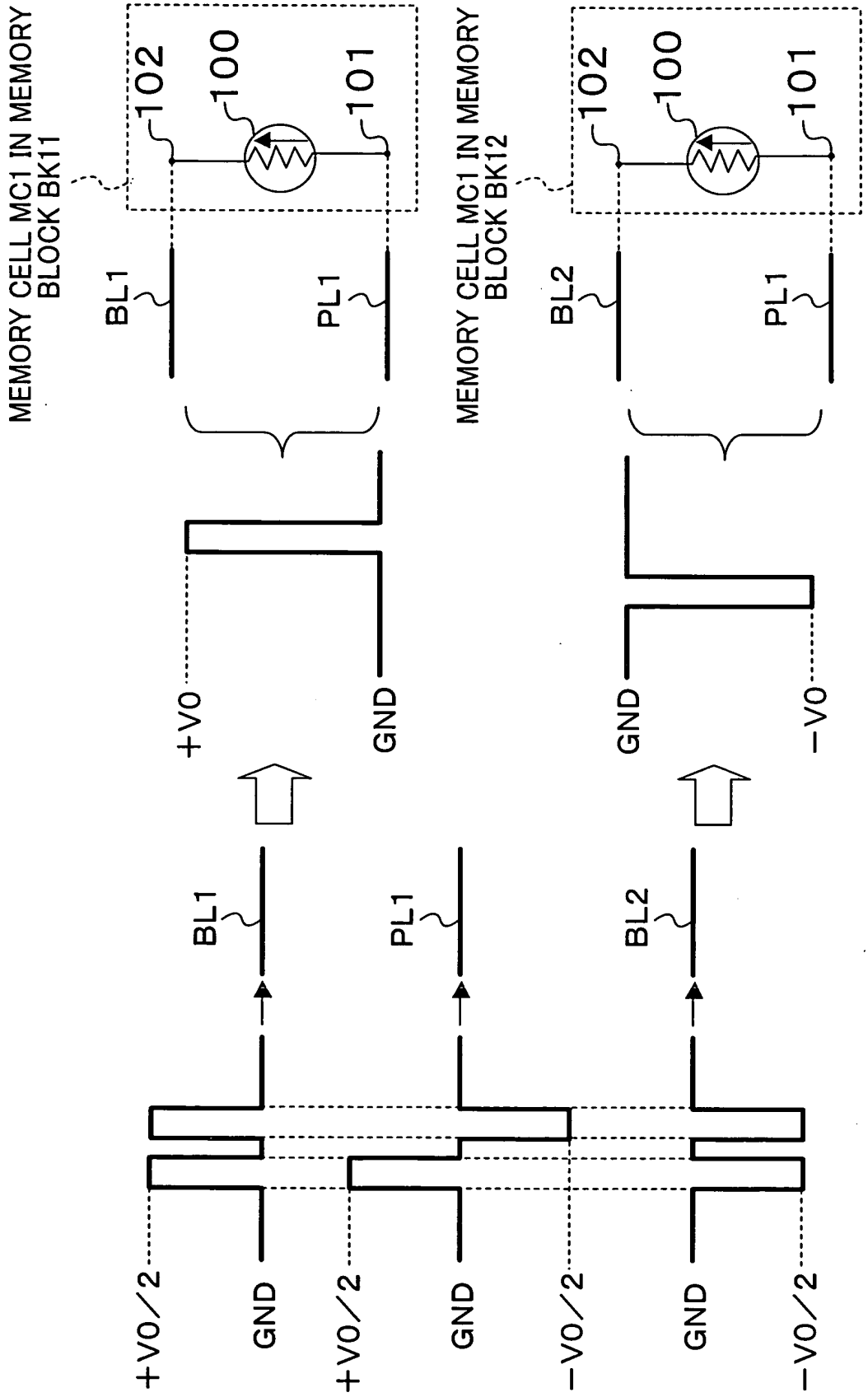

MEMORY CELL MC1 IN MEMORY BLOCK BK11
MEMORY CELL MC1 IN MEMORY BLOCK BK12
102
100
101
BL1
PL1
BL2
+V0
GND
−V0
+V0/2
−V0/2

FIG. 28

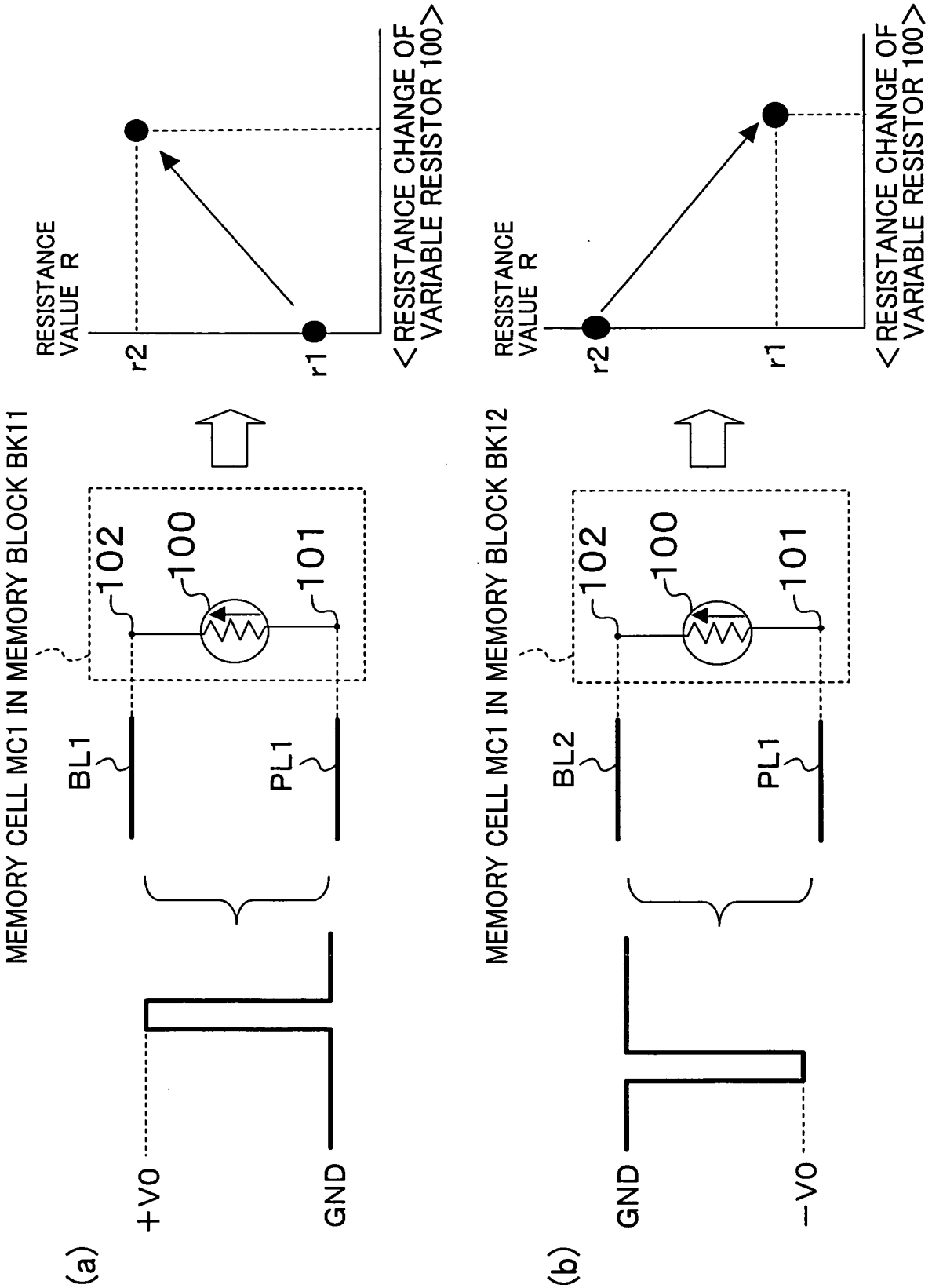

(a)
MEMORY CELL MC1 IN MEMORY BLOCK BK11
BL1
PL1
102
100
101
+V0
GND
RESISTANCE VALUE R
r2
r1
< RESISTANCE CHANGE OF VARIABLE RESISTOR 100 >
(b)
MEMORY CELL MC1 IN MEMORY BLOCK BK12
BL2
PL1
102
100
101
GND
−V0
RESISTANCE VALUE R
r2
r1
< RESISTANCE CHANGE OF VARIABLE RESISTOR 100 >

FIG. 29

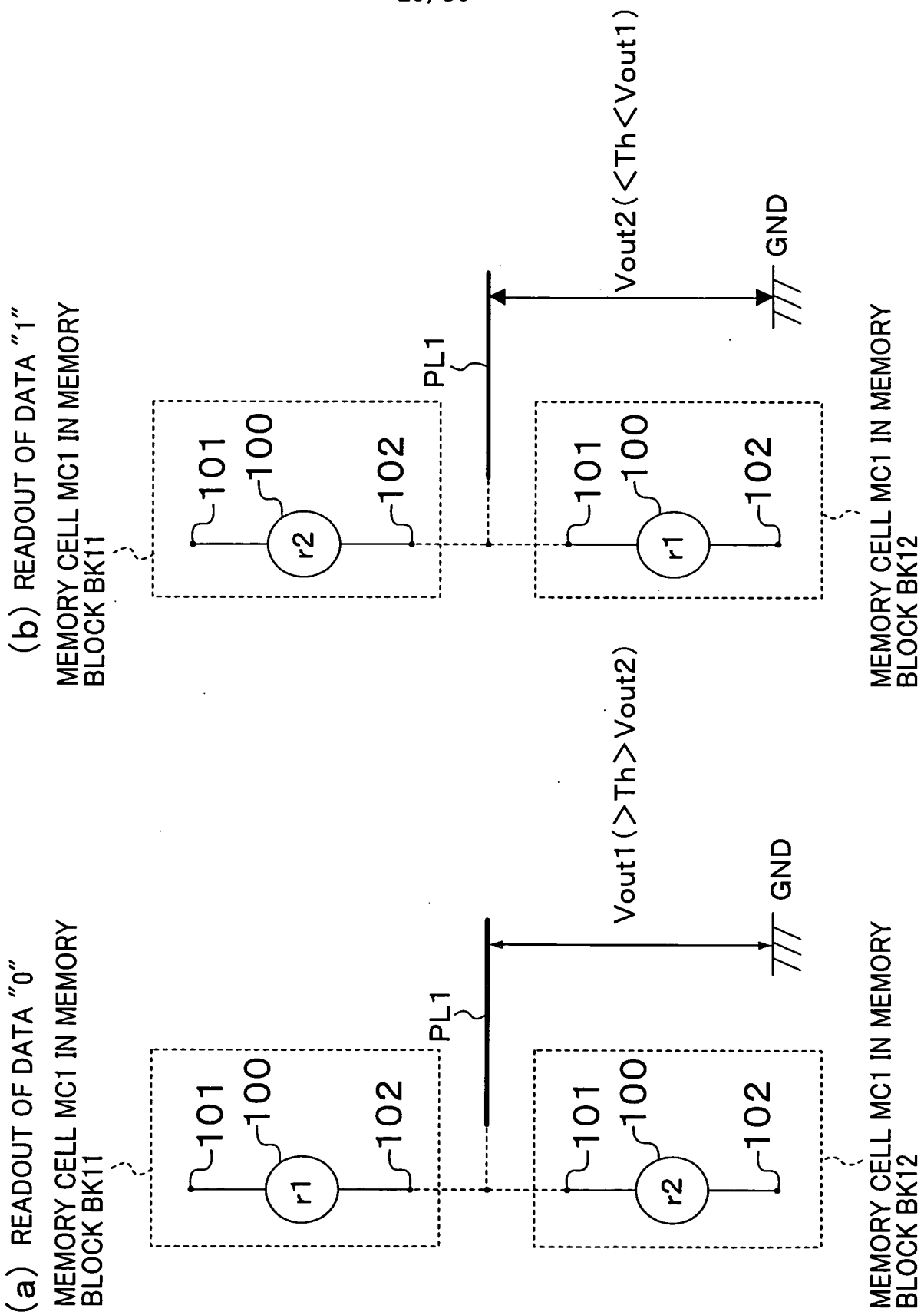

(a) READOUT OF DATA "0"
MEMORY CELL MC1 IN MEMORY BLOCK BK11
101
100
r1
102
PL1
Vout1 (>Th>Vout2)
GND
101
100
r2
102
MEMORY CELL MC1 IN MEMORY BLOCK BK12
(b) READOUT OF DATA "1"
MEMORY CELL MC1 IN MEMORY BLOCK BK11
101
100
r2
102
PL1
Vout2 (<Th<Vout1)
GND
101
100
r1
102
MEMORY CELL MC1 IN MEMORY BLOCK BK12

FIG. 30

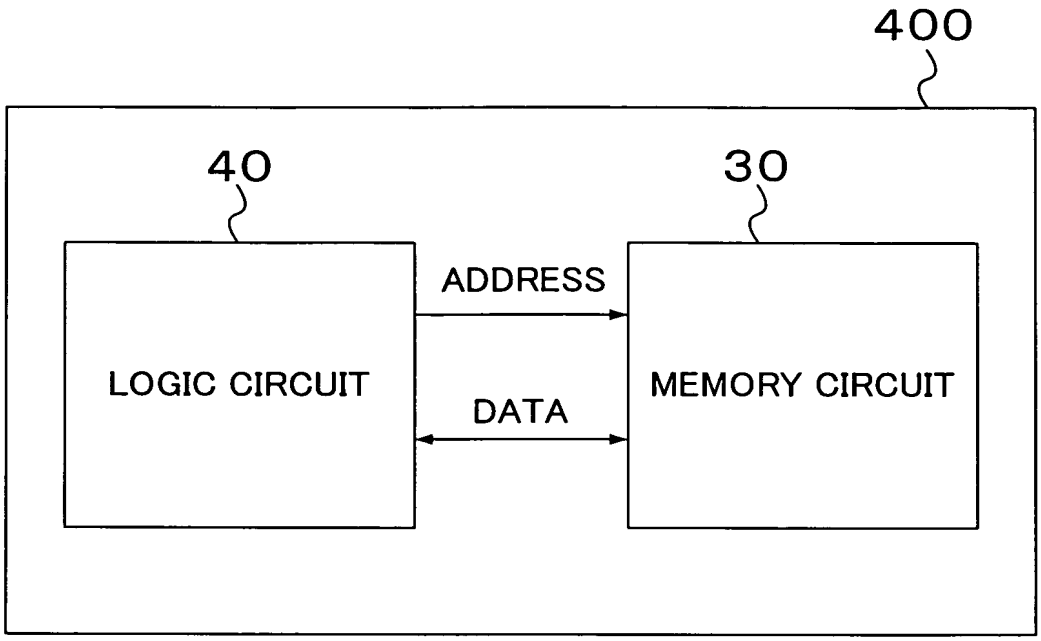
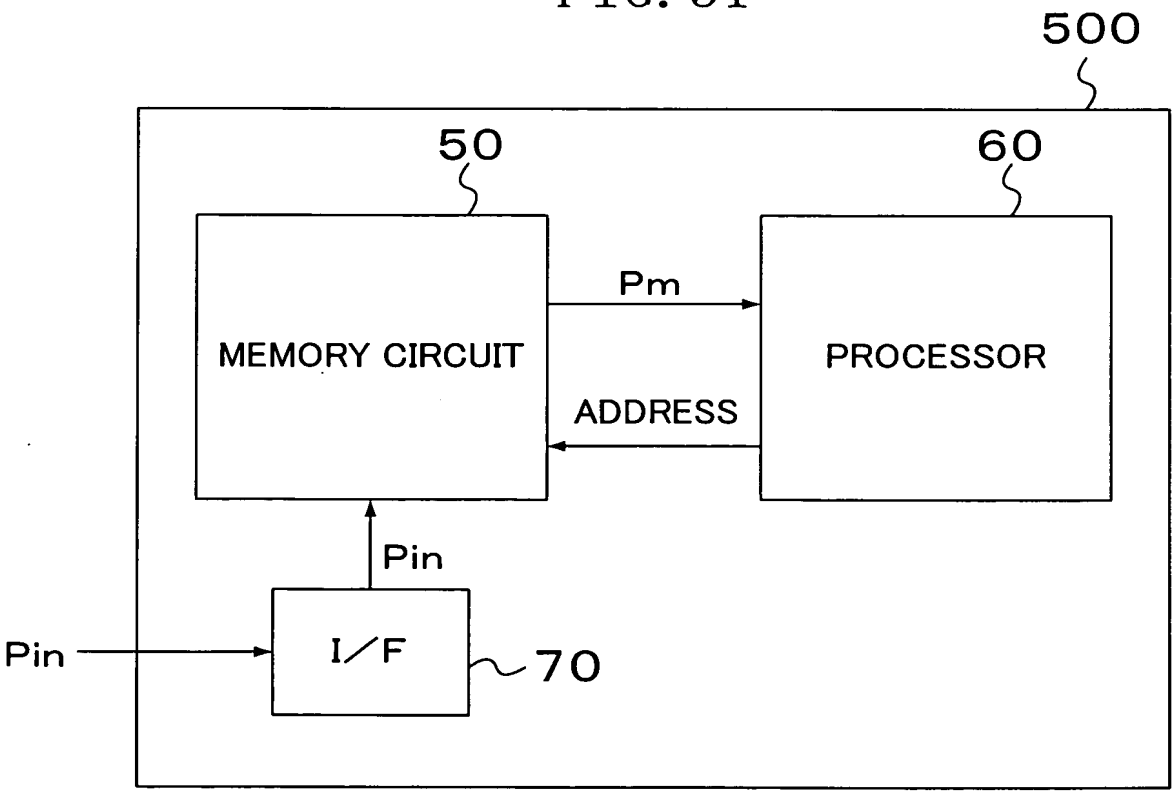

400
40
30
LOGIC CIRCUIT
ADDRESS
DATA
MEMORY CIRCUIT

FIG. 31


500
50
60
MEMORY CIRCUIT
Pm
ADDRESS
PROCESSOR
Pin
Pin
I/F
70